eBeam Initiative

Deep Learning (DL) Applications in Photomask to Wafer Semiconductor Manufacturing

Published by eBeam Initiative member companies (February 2024)

Company: Advantest Corporation

Product and/or Application

Mask metrology system
DL techniques used: Deep convolutional neural networks (DCNNs) and others
DL benefits: Processing speed and accuracy for image processing and defect recognition, with optimization for each application.

Company: ASML

Product and/or Application

Newron Model
DL techniques used: DCNNs
DL benefits: Significantly improves resist and etch model accuracy by capturing additional physical effects missed by conventional OPC models.

Newron SRAF
DL techniques used: DCNNs
DL benefits: Generates SRAF placements based on inverse OPC at full chip application speed, thus significantly improves process window at similar compute cost.

Newron OPC
DL techniques used: DCNNs
DL benefits: Accelerates OPC runtime significantly by reducing the number of iterations needed to achieve convergence.

Company: Canon

Product and/or Application

Auto alignment function in lithography tool
DL techniques used: Convolutional neural networks (CNNs) – VGGNet and transfer-learning are used
DL benefits: Reducing unscheduled downtime with judging alignment target image usability, better and quicker than humans.

Image processing and parameter tuning in lithography tool
DL techniques used: CNNs or region-based convolutional neutral networks (RCNNs)
DL benefits: Reducing optimization time and expansion of search area.

Deep Learning (DL) Applications in Photomask to Wafer Semiconductor Manufacturing

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Company: CEA-LETI

Product and/or Application

SEM image denoising
DL techniques used: Deep learning solution developed internally
DL benefits: Accuracy improvement, treatment speed.

Company: D2S

Product and/or Application

TrueMask® ILT GPU-accelerated, curvilinear full-chip ILT
DL techniques used: DCNNs and skip-connection (such as ResNet) based U-Net for the image-to-image translation
DL benefits: Speeds up full-chip ILT with a better starting point.

TrueMask DLK Quick start DL kit
DL techniques used: DCNN based deep Autoencoders (AE) for representing images
DL benefits: Robust deep learning applications created quickly with neural networks pre-trained for semiconductor manufacturing applications.

CD-SEM Digital Twins
DL techniques used: Generative Adversarial Networks (GAN), Neural Image Synthesis
DL benefits: Enables automated applications that analyze CD-SEM such as defect categorization, model extraction, etc.

Company: DNP

Defect classifier from inspection tool
DL techniques used: Deep convolutional neural networks (ResNet)
DL benefits: Improving processing speed and accuracy.

Improvement of pattern detection reliability
DL techniques used: Generative Adversarial Networks (GANs)
DL benefits: Image quality enhancement for reliable CD results.

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Company: Fraunhofer IPMS

Product and/or Application

Simultaneous contour edge image prediction and SEM image denoising (please refer to https://ieeexplore.ieee.org/abstract/document/9185250 joint paper with Texas A&M University)

DL techniques used: CNN LineNet2 trained with simulated training data set consisting of 32760 noisy SEM images with the corresponding original images and edge images
DL benefits: The method can be useful for real SEM image denoising, roughness estimation, and contour geometry estimation tasks.

Company: Hitachi High-Tech Corporation

Product and/or Application

Semiconductor wafer metrology and inspection system, image and data analysis system
DL techniques used: DCNNs, etc.
DL benefits: Image quality and throughput enhancement for metrology and inspection tool.

Company: Holon

Product and/or Application

Mask metrology system
DL techniques used: DCNNs, etc.
DL benefits: Improving processing speed and accuracy for the measurement of leading-edge masks such as ILT masks.

Company: imec

<u>Product and/or Application</u>

Deep learning for improved process window analysis
<u>DL techniques used</u>: Autoencoder Neural Network
<u>DL benefits</u>: Provides fast proxy for CD metrology defining process window for LS/CH/logic, etc. Improves classification for OPC metrology needs.

Deep learning for defect classification and detection
<u>DL techniques used</u>: Deep fully connected neural networks, DCNNs, Reinforcement Learning
<u>DL benefits</u>: Automatic localization and classification of defects in SEM images enabling enhanced defect inspection for aggressive pitches. Pitch and noise invariant.

Deep learning-based SEM image denoiser
<u>DL techniques used</u>: Deep fully connected neural networks, DCNNs
<u>DL benefits</u>: Unsupervised deep learning training scheme without requiring clean, noiseless images. Denoising reduces noise level only without altering the (real) information; no digital artefacts are introduced. Key process for working with thin resist or enabling contour detection capability.

Deep learning for predicting device electrical performance on metrology data
<u>DL techniques used</u>: Linear regression, Extra Tree Regressor, SVM
<u>DL benefits</u>: Analyzing the overlay data in semiconductor manufacturing and to make use of the overlay measurements from early steps in the process to predict electrical property of the final fabricated structures using machine learning techniques.

Federated machine learning for defect classification and detection
<u>DL techniques used</u>: Deep fully connected neural networks, DCNNs, Federated ML
<u>DL benefits</u>: Proposing a novel FedML framework, developing an improvised weight averaging algorithm against conventional FedAvg, towards supporting defect inspection for real world decentralized dataset from anonymous users.

Deep learning denoiser-assisted framework for robust SEM contour extraction for advanced semiconductor nodes
<u>DL techniques used</u>: Deep fully connected neural networks, DCNNs
<u>DL benefits</u>: Proposing a deep learning denoiser assisted framework for the extraction and analysis of SEM contours with a novel noise removal method, replacing conventional noise reduction techniques (as Gaussian/Median-blur, etc.) with efficacy in edge extraction accuracy, with minimum/no requirement of external user input or metadata to extract and analyze information from noisy SEM images. An improved contour extraction algorithm capable of extracting contours on the body of noisy raw image itself with a posteriori knowledge derived from its denoised twins.

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Company: NuFlare Technology, Inc.

Product and/or Application

SEM defect classifier
DL techniques used: DCNNs with ResNet, Pix2Pix and Cycle-GANs
DL benefits: Speed up the defect analysis and improve the classification accuracy. Defect analysis training, especially for novice engineers.

B-Spline Control Point generation tool
DL techniques used: CNN (U-net)
DL benefits: Infer control-point positions of unclamped b-spline curve in a shorter time.

Log analysis
DL techniques used: Natural Language Processing (NLP)
DL benefits: Automatically detects the abnormalities from log.

Beam drift prediction
DL techniques used: Long short-term memory (LSTM)
DL benefits: Improve mask drawing quality with automatic abnormal search and prediction.

Company: Siemens Industries Software, Inc.; Siemens EDA

Product and/or Application

Calibre Neural Network Assisted Modelling
DL techniques used: DCNN or DNN for predicting, post exposure, post development and post etch contours
DL benefits: Improves accuracy as well as predictability of the models.

Calibre Machine Learning OPC
DL techniques used: Deep Neural networks with supervised learning for speeding up OPC
DL benefits: Improvement in OPC speeds.

Calibre Machine Learning for SEM Image Processing
DL techniques used: DCNN for contour extraction, image filtering, and image pre-processing
DL benefits: Improved accuracy contour edge detection and contour extraction robustness.

Calibre Monotonic Machine Learning
DL techniques used: Feature vector driven neural networks for speedup of ILT for main features and SRAF insertion
DL benefits: Significant speedup of ILT.

Calibre LFD with Machine Learning
DL techniques used: Neural networks and data enrichment techniques for yield-limiters detection in the design flow
DL benefits: Order of magnitude speedup and improved coverage over standard techniques that result in improved design yield and reliability.

Calibre Wafer Defect Engineering with Deep Learning
DL techniques used: Feature vector driven neural networks for layout analysis and hotspot detection
DL benefits: Robust applications that speed up test chip development and improves yield and reliability in the fab by quickly and efficiently detecting yield limiter.

Calibre Fab Design Process co-optimization
DL techniques used: Fab data anchored data enrichment with GBT (Gradient Boosted Tree)
DL benefits: Robust handling of sparse fab metrology and inspection data. Fast feature importance ranking driving multivariable optimization.

Company: STMicroelectronics

Product and/or Application

Fab Digital Twin - automatic defect classification (ADC)
DL techniques used: CNNs
DL benefits: Corrective action in real time and defects are caught before other processes are added.

Company: Synopsys

Proteus Modeling
DL technique used: DCNNs to enhance resist and etch
DL benefits: Improved model quality with faster time to results.

S-Litho Modeling
DL technique used: CNN training based on synthetic rigorous data.
DL benefits: Full-chip speed capability based on predictive Resist 3D rigorous models for resist height, resist contours at various Z-Levels and stochastic failures.

Proteus Lithography Proximity Correction
DL technique used: DCNNs
DL benefits: Fewer correction iterations for faster convergence with comparable QoR.

Proteus AF Placement
DL technique used: DCNNs
DL benefits: Fast full chip curvilinear AF placement for improved wafer quality.

Proteus Litho/Etch Hotspot Detection
DL technique used: DCNNs
DL benefits: Improved detection of litho and non-litho related hotspots with comparable TAT.

Company: TASMIT

Product and/or Application

Semiconductor wafer metrology and inspection system
DL technique used: DCNNs for contour extraction and prediction in see-through image (HV-SEM BSE image)
DL benefits: Improving accuracy of contour extraction of underlayer pattern.

Semiconductor wafer metrology and inspection system
DL technique used: DCNNs for image denoising and super-resolution
DL benefits: Acceleration of inspection throughput.

Semiconductor wafer metrology and inspection system
DL technique used: Recurrent neural networks (RNNs) for modeling time-series data such as historical logs, the sequence of events
DL benefits: High-speed quantitative estimation of photo resist shrinkage, charging, etc.

Semiconductor wafer metrology and inspection system
DL technique used: Generative Adversarial Networks (GANs) to create new data including images, text, etc.
DL benefits: High speed and high accuracy for CAD based image processing, CAD to SEM contour matching, and defect inspection performance.

Semiconductor wafer metrology and inspection system
DL technique used: Anomaly detection using Gaussian Mixture Models (GMM), GANs to identify irregularities, undesirable patterns in the data
DL benefits: Simple parameter setting for defect inspection.

Semiconductor wafer metrology and inspection system
DL technique used: Extremely Randomized Trees (ERT) technology for the SEM contour extraction
DL benefits: High speed with lower cost of computer system for pattern edge detection.