



## **Deep Learning (DL) Applications in Photomask to Wafer Semiconductor Manufacturing**

Published by eBeam Initiative member companies (February 2025)

**Company: Advantest Corporation**

### **Product and/or Application**

#### **Mask metrology system**

DL techniques used: Deep convolutional neural networks (DCNNs) and others

DL benefits: Processing speed and accuracy for image processing and defect recognition, with optimization for each application.

**Company: ASML**

### **Product and/or Application**

#### **Newron Model**

DL techniques used: DCNNs

DL benefits: Significantly improves resist and etch model accuracy by capturing additional physical effects missed by conventional OPC models.

#### **Newron SRAF**

DL techniques used: DCNNs

DL benefits: Generates SRAF placements based on inverse OPC at full chip application speed, thus significantly improves process window at similar compute cost.

#### **Newron OPC**

DL techniques used: DCNNs

DL benefits: Accelerates OPC runtime significantly by reducing the number of iterations needed to achieve convergence.

**Company: Averroes.ai**

### **Product and/or Application**

#### **Smart Augmentation for Few-Shot Learning**

DL technique used: Vision Large Language Models (vLLMs), Generative Adversarial Networks (GANs), Diffusion Models

DL benefits:

- Context-aware augmentation strategies tailored to domain-specific data (e.g., medical, solar, semiconductor) while preserving semantic consistency via Diffusion Models.
- Utilizing vLLMs as logical elements that help us make contextual augmentation choices that portray the real-world use case.
- Using GANs to automate domain-specific environment transformations to the images as guided by vLLM logical elements.

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## **Automatic Deep Learning Model Architect**

DL Technique used: Vision Large Language Models (vLLMs), Vision Transformers (ViT), Convolutional Neural Networks (CNN)

DL Benefits:

- vLLM-guided architecture selection (ViTs, CNNs, ...) and hyperparameter tuning for optimized performance.
- Automated workflow management (data preprocessing, feature engineering, model evaluation) and explainability for debugging.
- Automated knowledge-based retrieval of image tokenization from relevant pre-trained models for domain-based knowledge transfer.

**Company: Canon**

## **Product and/or Application**

### **Auto alignment function in lithography tool**

DL techniques used: Convolutional neural networks (CNNs) – VGGNet and transfer-learning are used

DL benefits: Reducing unscheduled downtime with judging alignment target image usability, better and quicker than humans.

### **Image processing and parameter tuning in lithography tool**

DL techniques used: CNNs or region-based convolutional neural networks (RCNNs)

DL benefits: Reducing optimization time and expansion of search area.

**Company: CEA-LETI**

## **Product and/or Application**

### **Deep learning for 3D OPC**

DL techniques used: Image-to-image algorithm based on U-Net

DL benefits: Generation speed and wider variety of use cases

### **SEM image denoising**

DL techniques used: Deep learning solution developed internally

DL benefits: Accuracy improvement, treatment speed

### **CD-SEM Digital Twins**

DL techniques used: Image-to-image translation using Generative Adversarial Networks (GANs) and VAE

DL benefits: Generation speed, accuracy, adaptability to newer SEM device

### **Metrology data fusion**

DL techniques used: PCM and/or CNN with data from different metrology tools: AFM, CD-SEM, SAXS, OCD.

DL benefit: Accuracy, reliability, speed

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## Company: D2S

### Product and/or Application

#### **TrueMask® ILT GPU-accelerated, curvilinear full-chip ILT**

DL techniques used: DCNNs and skip-connection (such as ResNet) based U-Net for the image-to-image translation

DL benefits: Speeds up full-chip ILT with a better starting point.

#### **TrueMask DLK Quick start DL kit**

DL techniques used: DCNN based deep Autoencoders (AE) for representing images

DL benefits: Robust deep learning applications created quickly with neural networks pre-trained for semiconductor manufacturing applications.

#### **CD-SEM Digital Twins**

DL techniques used: Generative Adversarial Networks (GAN), Neural Image Synthesis

DL benefits: Enables automated applications that analyze CD-SEM such as defect categorization, model extraction, etc.

## Company: DNP

### Product and/or Application

#### **Defect classifier from inspection tool**

DL techniques used: Deep convolutional neural networks (ResNet)

DL benefits: Improving processing speed and accuracy.

#### **Improvement of pattern detection reliability**

DL techniques used: Generative Adversarial Networks (GANs)

DL benefits: Image quality enhancement for reliable CD results.

## Company: Fraunhofer IPMS

### Product and/or Application

**Simultaneous contour edge image prediction and SEM image denoising** (please refer to <https://ieeexplore.ieee.org/abstract/document/9185250> joint paper with Texas A&M University)

DL techniques used: CNN LineNet2 trained with simulated training data set consisting of 32760 noisy SEM images with the corresponding original images and edge images

DL benefits: The method can be useful for real SEM image denoising, roughness estimation, and contour geometry estimation tasks.

## Company: Hitachi High-Tech Corporation

### Product and/or Application

**Semiconductor wafer metrology and inspection system, image and data analysis system**

DL techniques used: DCNNs, etc.

DL benefits: Image quality and throughput enhancement for metrology and inspection tool.

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## Company: Holon

### Product and/or Application

#### **Mask metrology system**

DL techniques used: DCNNs, etc.

DL benefits: Improving processing speed and accuracy for the measurement of leading-edge masks such as ILT masks.

## Company: HOYA

### Product and/or Application

#### **Virtual metrology & Defect Classification**

DL techniques used: Deep-neural networks, including image deep convolutional neural networks (DCNNs).

DL benefits: Lowering defect identification and classification thresholds, improving processing speed and accuracy, and improving yield.

## Company: imec

### Product and/or Application

#### **Deep learning for improved process window analysis**

DL techniques used: Autoencoder Neural Network

DL benefits: Provides fast proxy for CD metrology defining process window for LS/CH/logic, etc. Improves classification for OPC metrology needs.

#### **Deep learning for defect classification and detection**

DL techniques used: Deep fully connected neural networks, DCNNs, Reinforcement Learning

DL benefits: Automatic localization and classification of defects in SEM images enabling enhanced defect inspection for aggressive pitches. Pitch and noise invariant.

#### **Deep learning-based SEM image denoiser**

DL techniques used: Deep fully connected neural networks, DCNNs

DL benefits: Unsupervised deep learning training scheme without requiring clean, noiseless images. Denoising reduces noise level only without altering the (real) information; no digital artefacts are introduced. Key process for working with thin resist or enabling contour detection capability.

#### **Deep learning for predicting device electrical performance on metrology data**

DL techniques used: Linear regression, Extra Tree Regressor, SVM

DL benefits: Analyzing the overlay data in semiconductor manufacturing and to make use of the overlay measurements from early steps in the process to predict electrical property of the final fabricated structures using machine learning techniques.

#### **Federated machine learning for defect classification and detection**

DL techniques used: Deep fully connected neural networks, DCNNs, Federated ML

DL benefits: Proposing a novel FedML framework, developing an improvised weight averaging algorithm against conventional FedAvg, towards supporting defect inspection for real world decentralized dataset from anonymous users.

# Deep Learning (DL) Applications in Photomask to Wafer Semiconductor Manufacturing

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## **Deep learning denoiser-assisted framework for robust SEM contour extraction for advanced semiconductor nodes**

DL techniques used: Deep fully connected neural networks, DCNNs

DL benefits: Proposing a deep learning denoiser assisted framework for the extraction and analysis of SEM contours with a novel noise removal method, replacing conventional noise reduction techniques (such as Gaussian/Median-blur, etc.) with efficacy in edge extraction accuracy, with minimum/no requirement of external user input or metadata to extract and analyze information from noisy SEM images. An improved contour extraction algorithm capable of extracting contours on the body of noisy raw image itself with a posteriori knowledge derived from its denoised twins.

## **EDA (Electronic Design Automation) Automation Using Deep Learning**

DL techniques used: LLM (Large Language models) finetuned on Skill code, Verilog/VHDL

DL benefits: proposing LLM based framework for automating standard cell placement & routing, modelling circuits as graph structures to predict optimal connectivity, fast power & delay estimation, design rule violation detection, to identify hotspots, OPC corrections and process variations.

## **Super-Resolution (SR) assisted framework towards increased SEM throughput for defect inspection**

DL techniques used: YOLO architecture with NAS (Neural-Architecture-Search) method integrated with a proposed Super-Resolution branch

DL benefits: proposed a SR-assisted framework towards increased SEM throughput ( $\sim x8$ ) for defect inspection, by reduction of required SEM image pixel resolutions. Proposed framework demonstrates improved defect inspection performance/precision for acquired SEM images from different tools (SEM/EDR) and different process steps (ADI/AEI) at lower resolutions/FoV. Additionally proposed novel data augmentation strategies (SEM specific), and their contribution to enhance generalizability and robustness.

## **GenAI based SEM image generation to address class imbalance and training data insufficiency in advanced node semiconductor defect inspection**

DL techniques used: Diffusion model, inpainting method, DCNNs, etc.

DL benefits: Proposed a patch-based generative framework utilizing DDPM towards generating synthetic SEM images while preserving metrology specifications of real images. Defect detector models were trained and benchmarked on these generated synthetic images under different conditions to further validate the applicability of synthetic images within a robust defect inspection framework. Proposed framework can be trained on different processes and their associated defect types concurrently. Proposed framework can generate defect types outside its typical process parameters, to prepare defect detectors for unexpected scenarios, to support defect transfer.

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**Company:** NuFlare Technology, Inc.

## Product and/or Application

### **SEM defect classifier**

DL techniques used: Deep convolutional neural networks with ResNet, Pix2Pix and Cycle-GANs

DL benefits: Speed up the defect analysis and improve the classification accuracy. Defect analysis training, especially for novice experts.

### **B-Spline Control Point generation tool**

DL techniques used: Convolutional neural network (U-net)

DL benefits: Infer control-point positions of unclamped b-spline curve in a shorter time.

### **Log analysis**

DL techniques used: Natural Language Processing (NLP)

DL benefits: Automatically detect the abnormalities from log.

### **Beam drift Prediction**

DL techniques used: Long short-term memory (LSTM)

DL benefits: Improve mask drawing quality with automatic abnormal search and prediction.

### **Equipment health check and Prediction**

DL techniques used: Long short-term memory (LSTM)

DL benefits: Automated and fast analysis with over 100 measured parameters.

**Company:** Siemens Industries Software, Inc.; Siemens EDA

## Product and/or Application

### **Calibre Neural Network Assisted Modelling**

DL techniques used: DCNN or DNN for predicting, post exposure, post development and post etch contours

DL benefits: Improves accuracy as well as predictability of the models.

### **Calibre Machine Learning OPC**

DL techniques used: Deep Neural networks with supervised learning for speeding up OPC

DL benefits: Improvement in OPC speeds.

### **Calibre Machine Learning for SEM Image Processing**

DL techniques used: DCNN for contour extraction, image filtering, and image pre-processing

DL benefits: Improved accuracy contour edge detection and contour extraction robustness.

### **Calibre Monotonic Machine Learning**

DL techniques used: Feature vector driven neural networks for speedup of ILT for main features and SRAF insertion

DL benefits: Significant speedup of ILT.

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## **Calibre LFD with Machine Learning**

DL techniques used: Neural networks and data enrichment techniques for yield-limiters detection in the design flow

DL benefits: Order of magnitude speedup and improved coverage over standard techniques that result in improved design yield and reliability.

## **Calibre Wafer Defect Engineering with Deep Learning**

DL techniques used: Feature vector driven neural networks for layout analysis and hotspot detection

DL benefits: Robust applications that speed up test chip development and improves yield and reliability in the fab by quickly and efficiently detecting yield limiter.

## **Calibre Fab Design Process co-optimization**

DL techniques used: Fab data anchored data enrichment with GBT (Gradient Boosted Tree)

DL benefits: Robust handling of sparse fab metrology and inspection data. Fast feature importance ranking driving multivariable optimization.

**Company: STMicroelectronics**

### **Product and/or Application**

#### **Fab Digital Twin - automatic defect classification (ADC)**

DL techniques used: CNNs

DL benefits: Corrective action in real time and defects are caught before other processes are added.

**Company: Synopsys**

### **Product and/or Application**

#### **Proteus Modeling**

DL technique used: DCNNs to enhance resist and etch

DL benefits: Improved model quality with faster time to results.

#### **S-Litho Modeling**

DL technique used: CNN training based on synthetic rigorous data.

DL benefits: Full-chip speed capability based on predictive Resist 3D rigorous models for resist height, resist contours at various Z-Levels and stochastic failures.

#### **Proteus Lithography Proximity Correction**

DL technique used: DCNNs

DL benefits: Fewer correction iterations for faster convergence with comparable QoR.

#### **Proteus AF Placement**

DL technique used: DCNNs

DL benefits: Fast full chip curvilinear AF placement for improved wafer quality.

#### **Proteus Litho/Etch Hotspot Detection**

DL technique used: DCNNs

DL benefits: Improved detection of litho and non-litho related hotspots with comparable TAT.

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**Company: TASMIT**

## **Product and/or Application**

### **Semiconductor wafer metrology and inspection system**

DL technique used: Combination of DCNNs and ACM (Active Contour Model) for contour extraction and prediction in see-through image (HV-SEM BSE image)

DL benefits: Improving accuracy of contour extraction of underlayer pattern.

### **Semiconductor wafer metrology and inspection system**

DL technique used: DCNNs for image denoising and super-resolution

DL benefits: Acceleration of inspection throughput.

### **Semiconductor wafer metrology and inspection system**

DL technique used: Generative Adversarial Networks (GANs) to create new data including images, text, etc.

DL benefits: High speed and high accuracy for CAD based image processing, CAD to SEM contour matching, and defect inspection performance.

### **Semiconductor wafer metrology and inspection system**

DL technique used: Extremely Randomized Trees (ERT) technology for the SEM contour extraction

DL benefits: High speed with lower cost of computer system for pattern edge detection.