Beam
Initiative

eBeam Initiative

5th Annual eBeam Initiative Luncheon

SPIE – February 26, 2013

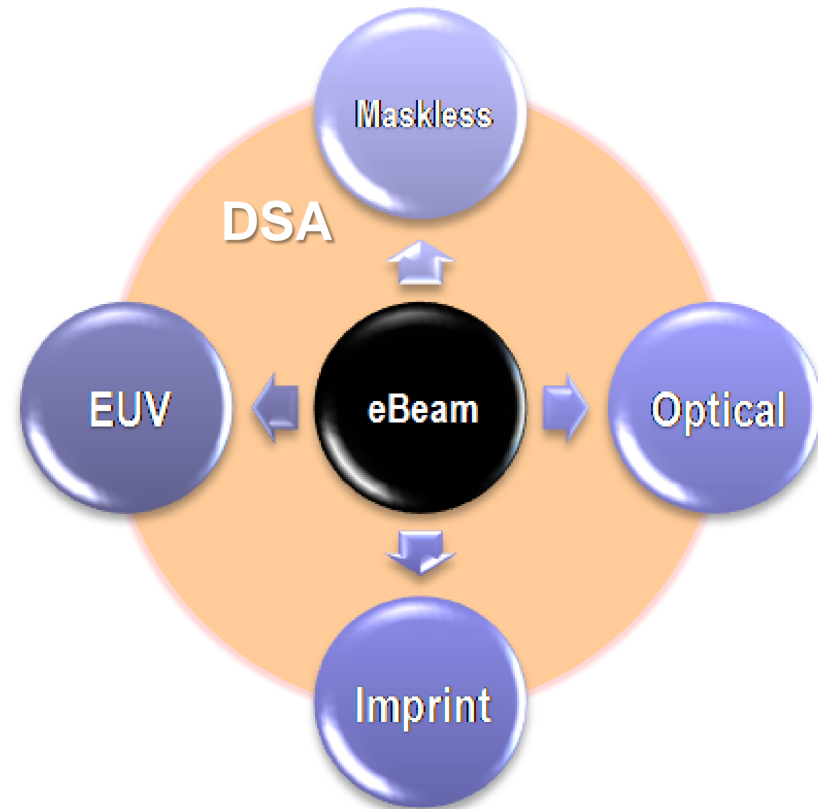
Aki Fujimura
CEO – D2S, Inc.
Managing Company Sponsor – eBeam Initiative

eBeam Writes All Chips

eBeam Initiative

The eBeam Initiative:

- Is an educational platform for eBeam technology and its impact on all lithography approaches
- Open to any company in the semiconductor design chain with an interest in eBeam technologies



44 Member Companies & Advisors

www.ebeam.org

John Chen
NVIDIA

Grenon Consulting

Colin Harris
PMC-Sierra

Riko Radojcic
Qualcomm

Jean-Pierre Geronimi
ST

Hugh Durdan
Xilinx

Two Industry Veterans Join as eBeam Initiative Advisors

Hugh Durdan
Xilinx

John Chen
NVIDIA

New: The Fine Line Video Journal
Use your new earphones!

eBeam Initiative

Winter 2013 Edition

Shot Talk:
D2S

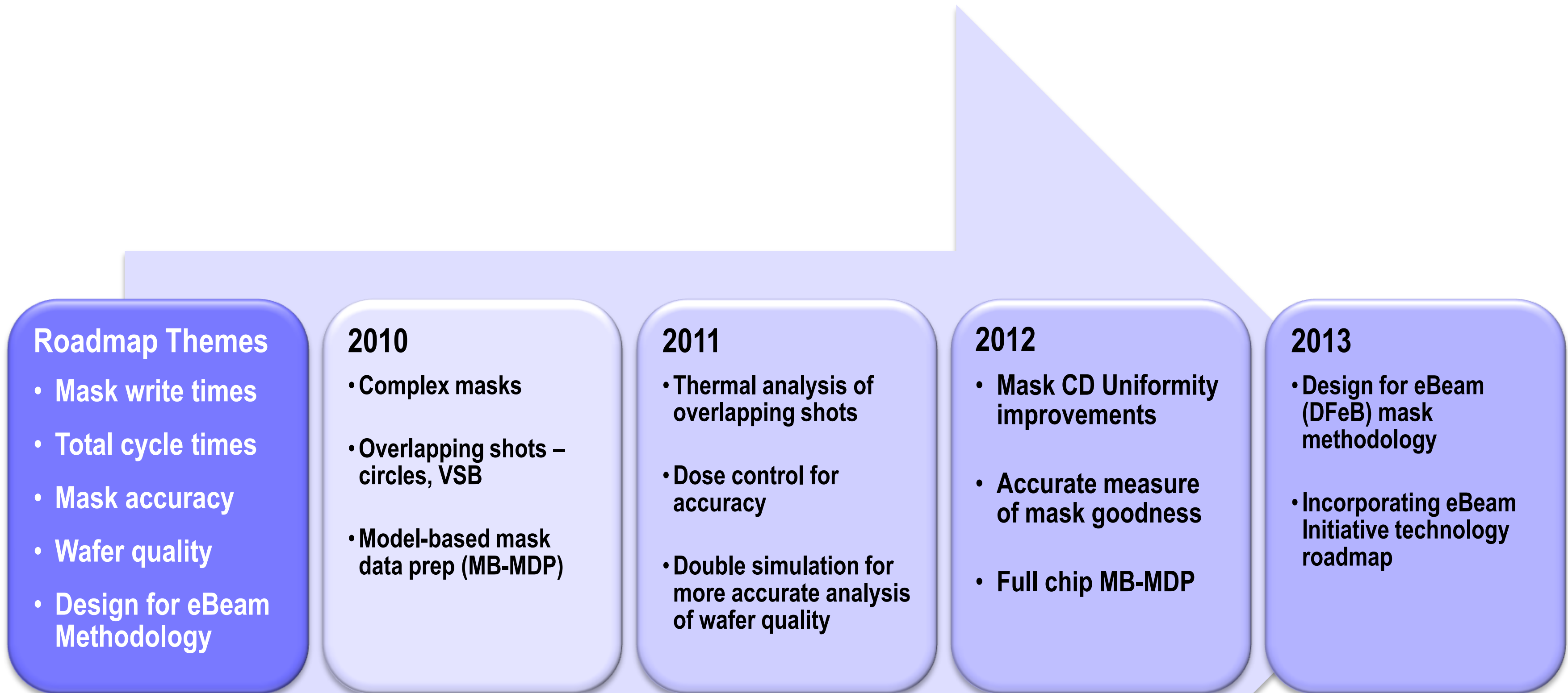
From the White Board:
Ryan Pearman

Tech Talk:
Samsung & D2S

$$eMEEF = N \frac{\Delta CDwafer}{\Delta eBeamDose}$$

Perspectives:
Hugh Durdan, Xilinx

Design for eBeam (DFeB) Roadmap



Wafer Process Enhanced by eBeam

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- More Complex Shapes on mask enhance Wafer Process Latitude
- Complex Masks, Manhattanized or ideal curvilinear, had two problems:
    - Poor mask CDU leading to unreliable results on wafer
    - Mask write time
- Samsung and GLOBALFOUNDRIES studies show MB-MDP solves this problem

Source: Samsung and D2S at BACUS 2012

Multibeam Technology Progress

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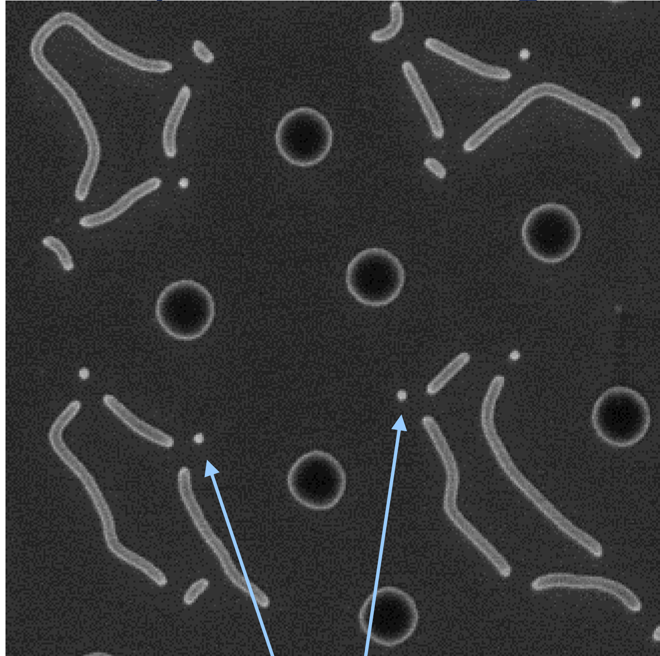
eMET POC exposure with 256k-APS ILT device test pattern

ILT device
test pattern

Design: DNP

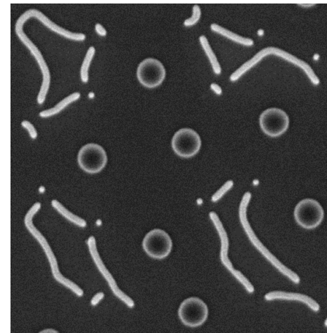
Scanning Stripe exposure	20nm beam size	5nm pixel size	with PEC

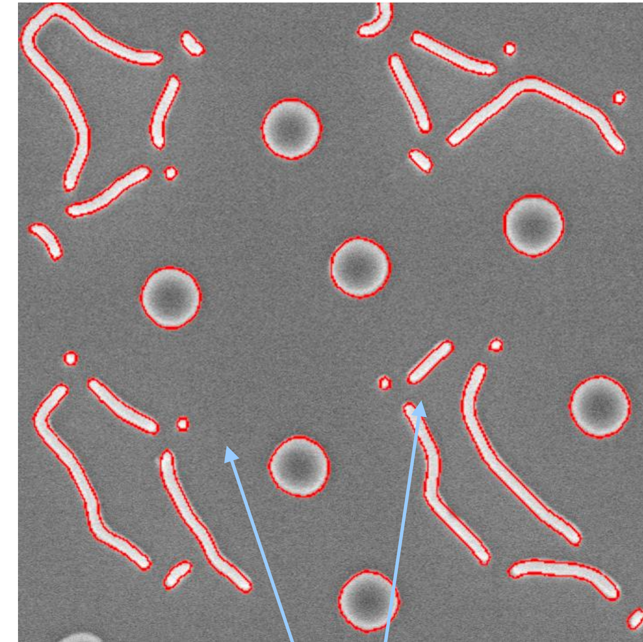
exposure of DNP design



60nm dots

exposure 2-times smaller





Design

30nm dots

Source: IMS Nanofabrication at BACUS 2012

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Our Next Speakers

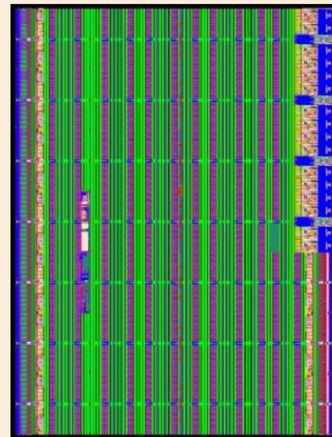
- **Chip Design Perspective**
  - Hugh Durdan, Xilinx
- **DSA Technology Challenges**
  - Dr. Tatsuhiko Higashiki, Toshiba
- **Q&A**

Lithography Challenges in Advanced Nodes – A Design Perspective

Hugh Durdan
Vice President, Portfolio & Solutions Marketing

The 'Chameleon' Chip

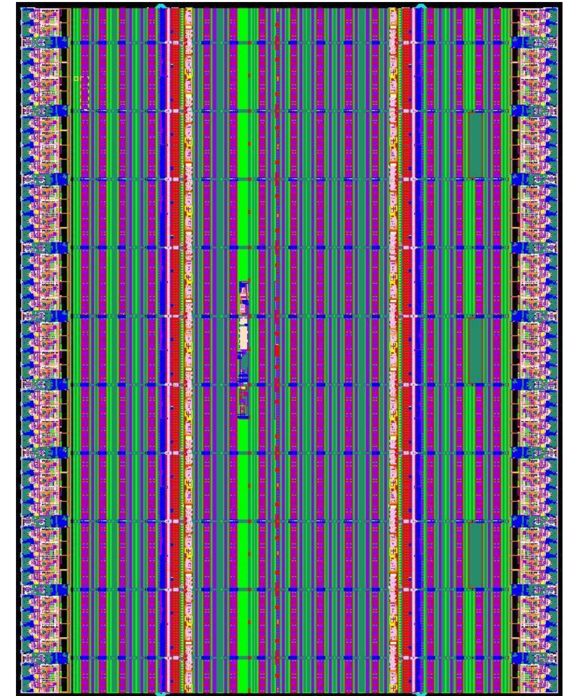
Field Programmable Gate Array (FPGA)



XILINX ➤ ALL PROGRAMMABLE.

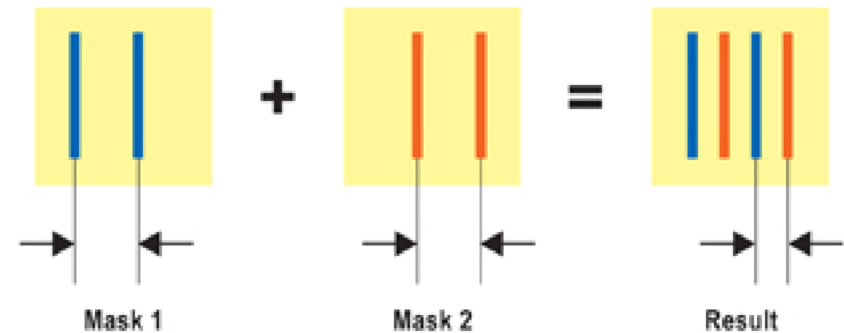
FPGA Characteristics

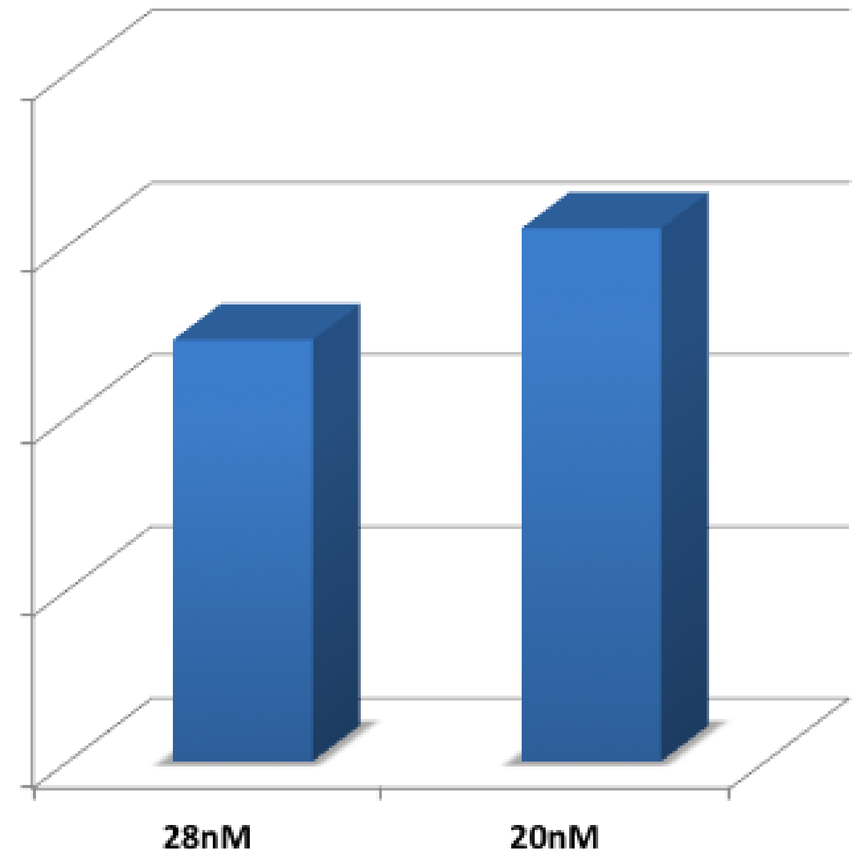
- **Large devices**
  - Often > 400mm2
  - Up to 7 billion transistors
- **Regular structures**
  - Ideal for driving process maturation
- **Historically benefitted from Moore's Law**
  - Insatiable demand for more capabilities & capacity
  - Until 20nM, process scaling has offered higher performance, lower power, and lower cost at each successive node



So What's Changed?

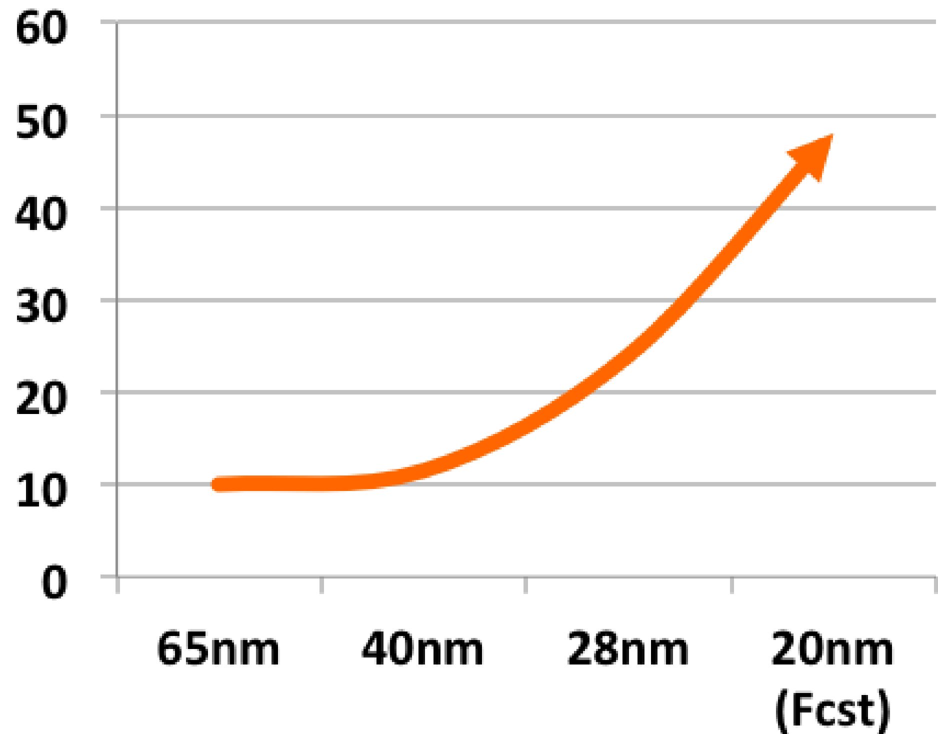
- More complex transistor structure = more masks
- Double patterning required for finer features in 20nM = more masks
- Net result is 30% increase in masking layers
- Directly translates into increased mask and wafer costs





And Even Worse…

- **Mask write time increases exponentially**
  - Reduced throughput
  - Higher cost per mask
- **More restrictive design rules**
  - Larger die
- **Reduced CD uniformity**
  - More design margin
  - Lower yields



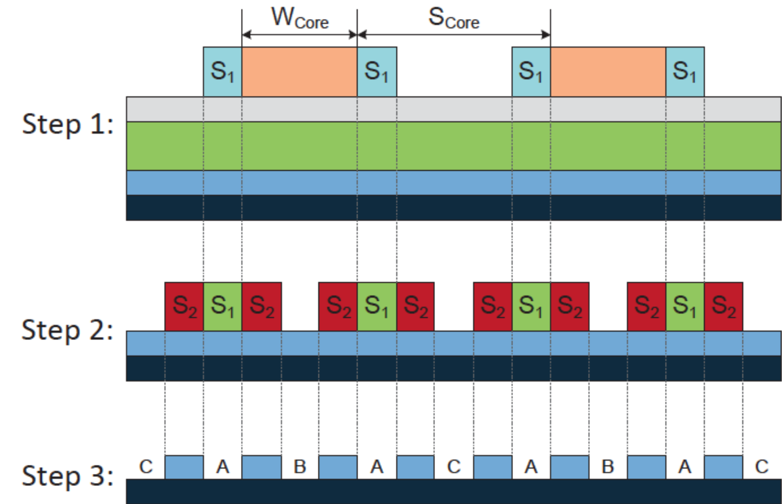
Max. Mask Write Time (Hours)

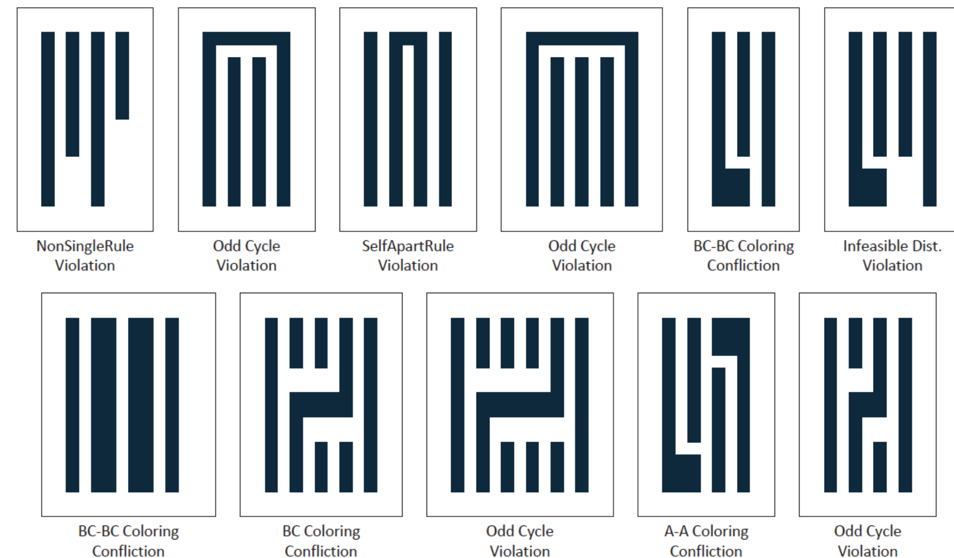
What Happens at 16/14nM?

- **The Good**
  - Higher performance or lower power
    - *But not both…*
- **The Bad**
  - Interconnect pitch same as 20nM
    - *So no die shrink…*
- **The Ugly**
  - Even more restrictive design rules
    - *Die size could grow!*
  - More mask layers
    - *Fin-FET structure & double patterning*
  - Lower yields

10nM & Beyond: Quadruple Patterning

- "Double Double"
- Extends life of existing infrastructure
  - 193nM light sources & immersion lithography
- Only a stop-gap for 10nM
- Alignment becomes a significant issue
- Even more restrictive design rules
- More masks = increased mask and wafer costs

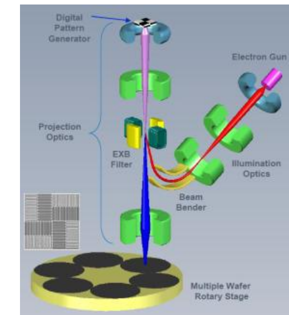




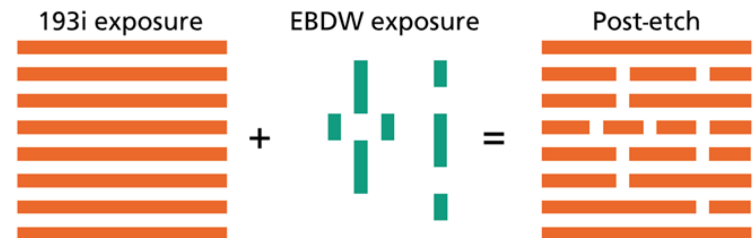
Other Possibilities Xilinx is Watching

- EUV
- EBDW
- Hybrid Approach
- Directed Self-Assembly

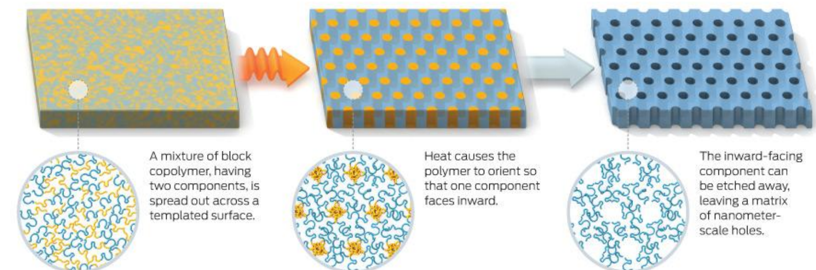
Source: ASML



Source: KLA-Tencor



Source: Intel



Source: IEEE Spectrum

Perspectives

- **Lithography challenges are a significant threat to maintaining Moore's Law**
- **Cost per transistor is going up for the first time in the history of the semiconductor industry**
- **No good solution on the horizon**
  - Quadruple patterning only good in the short-term
  - EUV immature, expensive, and late
  - Direct-write too slow today for volume production
- **eBeam will be part of the solution**
  - Better accuracy in mask making to reduce CD variation
  - Hybrid approach
  - Direct write if throughput can be improved

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DSA Technology Challenges

Center for Semiconductor Research & Development
Advanced Lithography Process Technology Dept.

Tatsuhiko Higashiki

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Lithography Challenges

More Moore

hp56nm hp43nm hp32nm hp2xnm hp1xnm hp0xnm

More than Moore

Light Source

Resist, Mask, Inspection, etc

Cost

Defect

Tool

EUVL NA0.32→ >0.4x ?

EUVL+SADP

EUVL+DSA

ArF im NA>1~1.35

ArF im SADP

ArF imSAQP/SAOP ?

Arf im SAQP+DSA

NIL

NIL+DSA

ML2

ML2+DSA

Performance & Economics

SADP : self-aligned double patterning
SAQP : self-aligned quadruple patterning
SAOP : self-aligned octuplet patterning

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DSAL *(Directed Self Assembly Lithography)*

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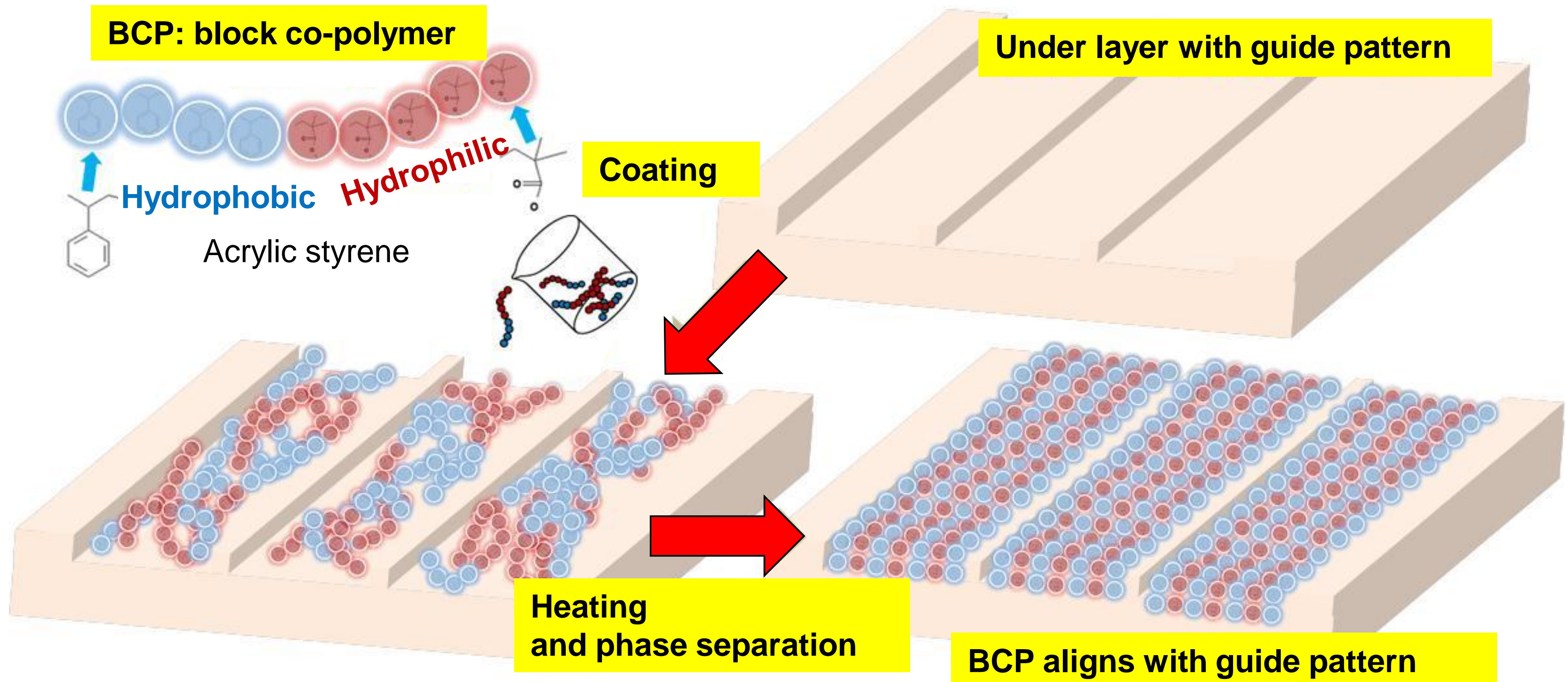
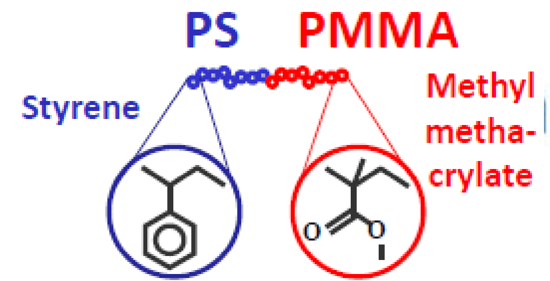
Lithography of using self-organization phenomenon of polymer

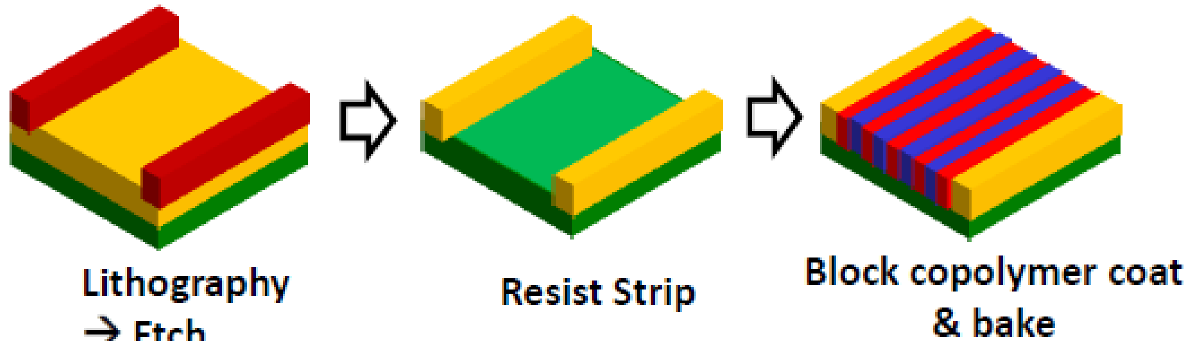


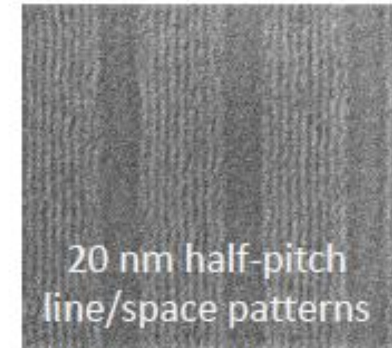
Grapho-Epitaxy & Chemo-Epitaxy



Grapho-Epitaxy

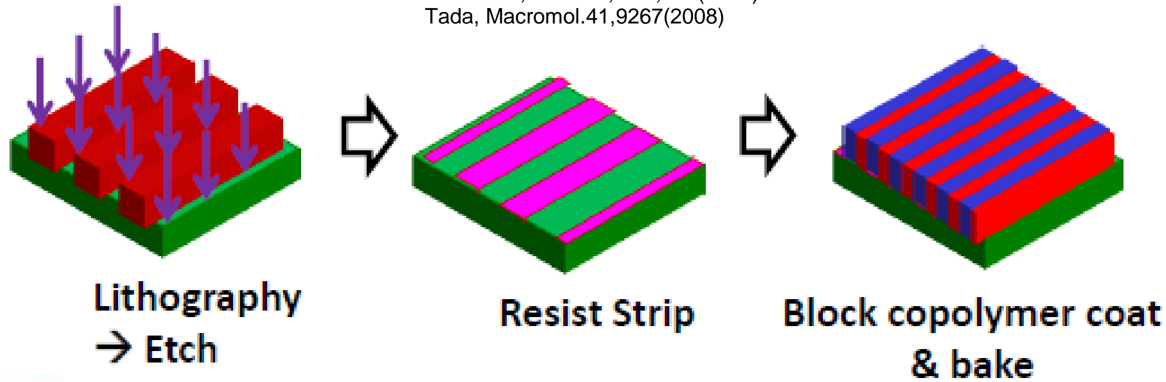
Segalmann et al., *Adv.Mater.* 3,1152(2001)
Nato et al., *IEEE Trans. Magn.*38,1949(2002)
Chen et al.,Appl.Phys.Lett.81,3657(2002)

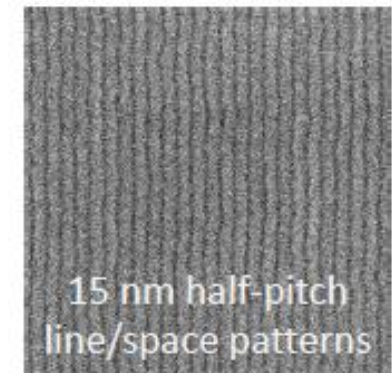




Chemo-Epitaxy

Chen et al.,*Adv.Mater.* 20,3155(2008)
Rulz et al., *Science, 321,936*(2008)
Tada, Macromol.41,9267(2008)



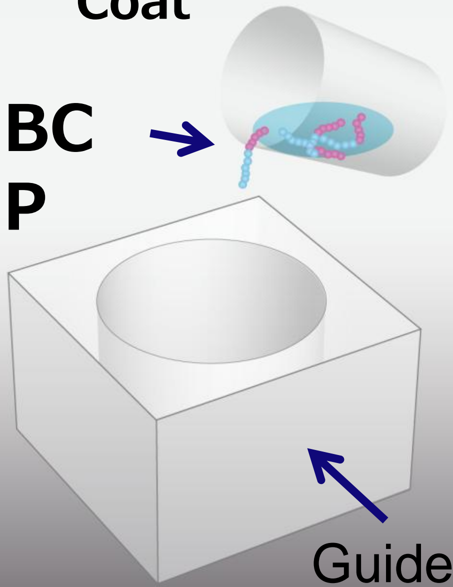


DSA L for Contact Hole Pattern

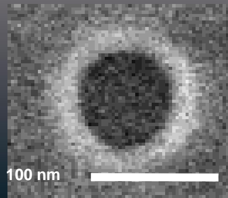
Process Flow of DSA Lithography

1 BCP Coat

BC
P

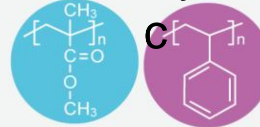


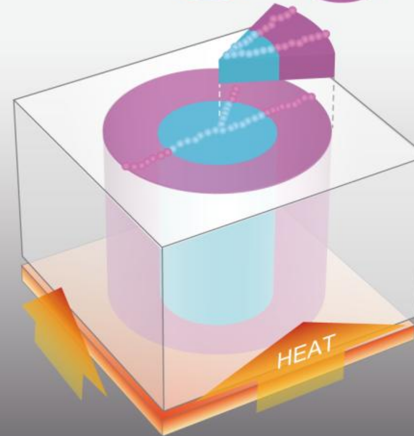
Guide



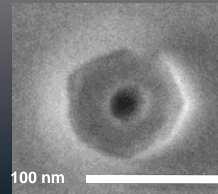
2 Annealing

Hydrophilic Hydrophobi
c

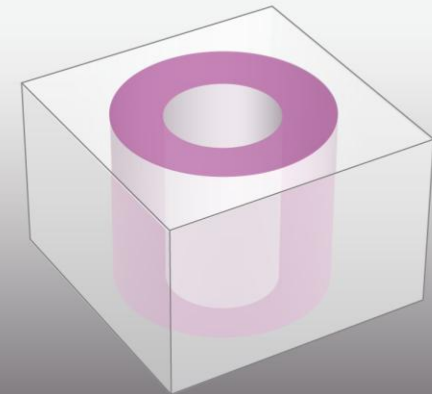


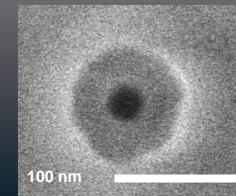


DSA



3 Development





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DSA OPC/DfM/APC Flow

OPC

DSA DRC?

Layout

Guide Data

EDA Tool

Guide OPC Spec/Verification 5x ?

OPC

Guide Data Preparation TAT x 1M?

Litho Simulation

DfM

GDS

Sim TAT x 10k

Model

DSA Simulation

FeedBack

Accuracy x 20

HotSpot result

EDA Tool

Condition (material/process)

Judge

APC

Wafer Process

FeedForward

3D Metrology & Inspection

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Example of DPD Simulation

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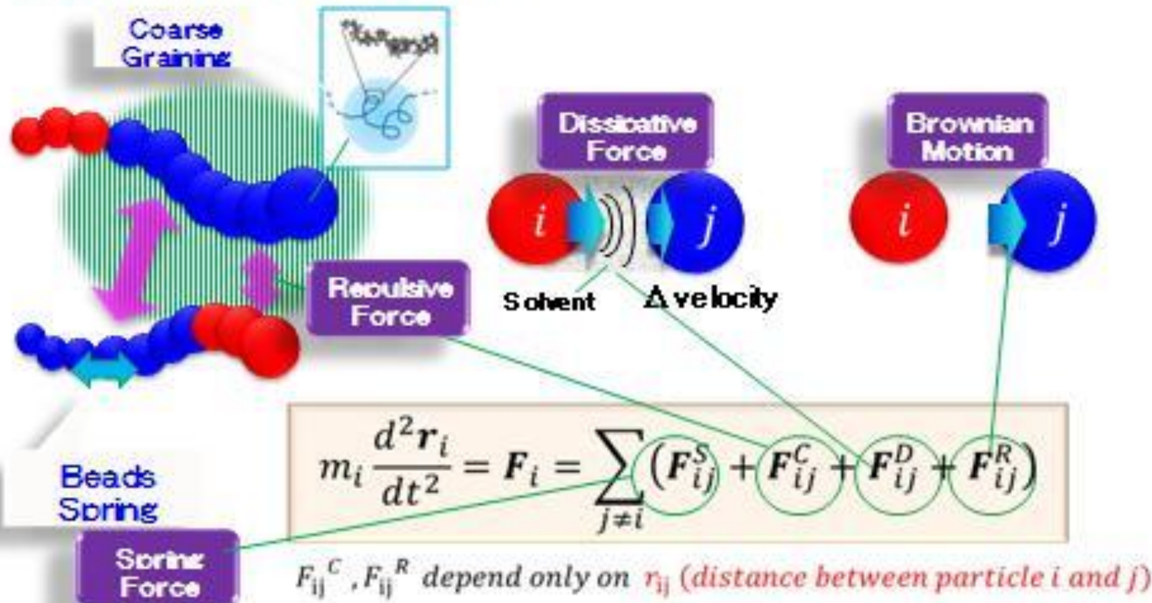

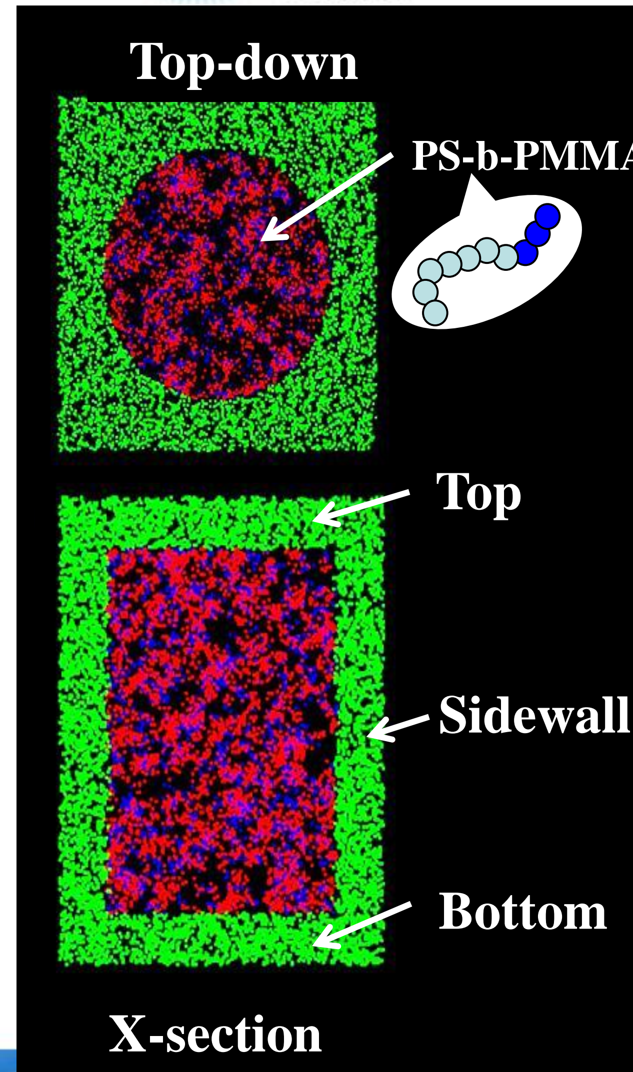

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DSA Simulation Model

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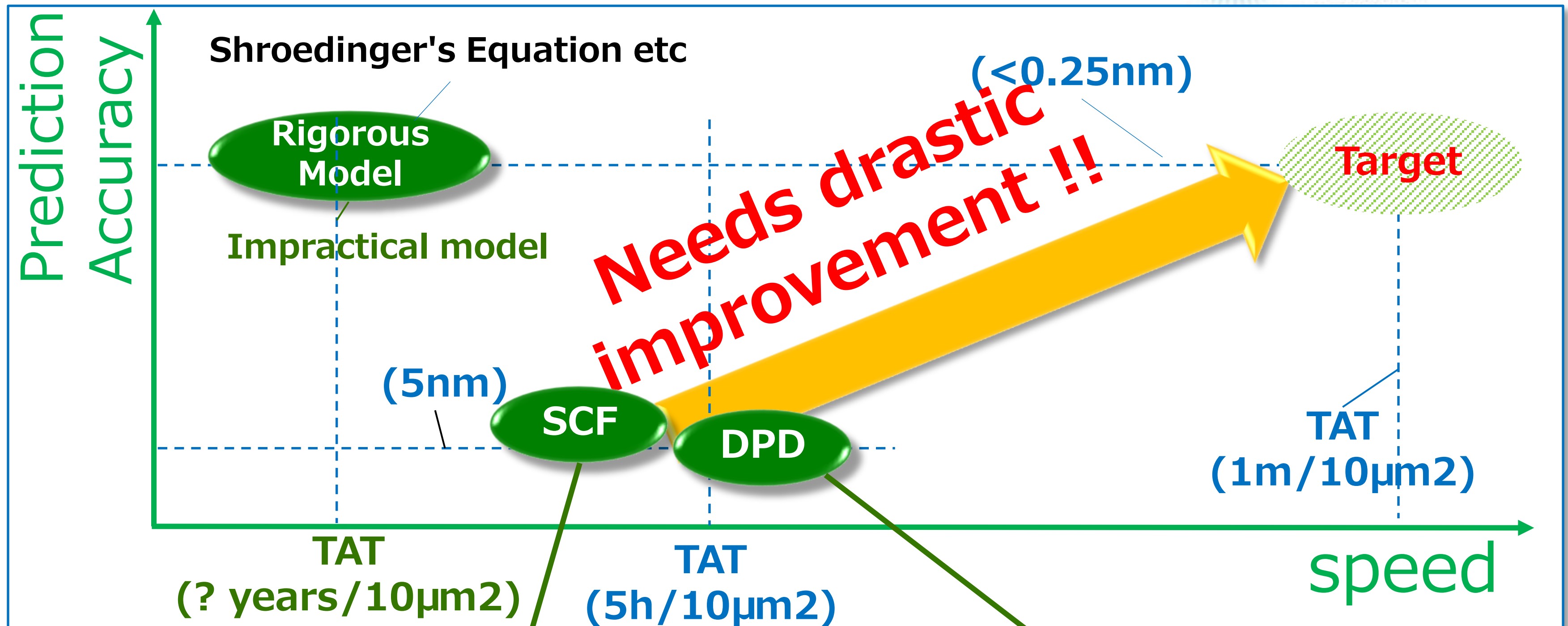

Model	Self Consistent mean Field	Dissipative Particle Dynamics
methodology	Based on statistical field theory	Based on Newton's motion equation
Challenge	Modeling of thermal fluctuations	Difficult to fit to a measured data

Conclusion: Challenges for DSAL

- High performance DSA material
  - Resolution, LWR/LER, Etching
- Long term stability
  - Robust material and tool for environmental control such as surface energy stability, temperature, humidity, pressure and PH, etc.
  - Defectivity, CD and overlay accuracy
- Metrology & Inspection
  - Metrology for 3D profile
  - Inspection technology for 1xnmhp and beyond needs to overcome t-put vs accuracy/sensitivity trade-off.
- Development of molecular dynamics based DSA simulator
  - More accurate simulation model
    - BCP and related molecular design
    - Microphase separation (2D/3D)
    - DSA and guide patterning (litho/wet/dry)
  - TAT vs accuracy trade-off
- DSA OPC/DFM technology
  - Design rule verification

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Thank you for attending!

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Q & A

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