Cell projection use in mask-less lithography for 45nm & 32nm logic nodes

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ABSTRACT

Due to the ever-increasing cost of equipment and mask complexity, the use of optical lithography for integrated circuit manufacturing is increasingly more complex and expensive. Recent workshops and conferences in semiconductor lithography underlined that one alternative to support sub-32nm technologies is mask-less lithography option using electron beam technology. However, this direct write approach based on variable shaped beam principle (VSB) is not sufficient in terms of throughput, i.e. of productivity. New direct write techniques like multibeam systems are under development, but these solutions will not be mature before 2012. The use of character/cell projection (CP) on industrial VSB tools is the first step to deal with the throughput concerns. This paper presents the status of the CP technology and evaluates its possible use for the 45nm and 32nm logic nodes. It will present standard cell and SRAM structures that are printed as single characters using the CP technique. All experiments are done using the Advantest tool (F3000) which can project up to 100 different cells per layer. Cell extractions and design have been performed with the design and software solution developed by D2S. In this paper, we first evaluate the performance gain that can be obtained with the CP approach compared to the standard VSB approach. This paper also details the patterning capability obtained by using the CP concept. An evaluation of the CD uniformity and process stability is also presented. Finally this paper discusses about the improvements of this technique to address high resolution and to improve the throughput concerns.

Keywords: electron beam, cell projection, design, resolution, proximity effects, direct write, NGL

1. INTRODUCTION

Recent workshops and conferences in semiconductor lithography underlined that one alternative to support sub-32nm technologies is the mask-less lithography option using electron beam direct write technology [1]. The direct write approach based on variable shaped beam principle (VSB) has proven its advantages for advanced patterning applications, prototyping and small volume production. It also allows a great flexibility for fast turnaround times and even late design modifications to correct or adapt a given chip layout. The direct write approach based on variable shaped beam principle (VSB), however, is not sufficient in terms of throughput, i.e. of productivity. New direct write techniques like multibeam systems [2] are under development, but these solutions will not be mature before 2012. The use of character/cell projection (CP) [3, 4] on industrial VSB tools is the first step to deal with the throughput concerns.

This paper presents the cell projection concept using Advantest F3000 last generation variable shaped beam tool for patterning. The status of the CP technology and its possible use for the 45nm and 32nm logic nodes is studied. It also details the patterning results of

advanced standard cell and SRAM structures exposed as single characters using the CP technique. All experiments are done using the F3000 Advantest tool which can project up to 100 different cells per layer. Cell extractions and design have been performed with the design and software solution developed by D2S. In this paper, we first evaluate the performance gain that can be obtained with the CP approach compared to the standard VSB approach. This paper also highlights the patterning capability of structures down to 32nm design rules obtained by using the CP concept. An evaluation of the CD uniformity, energy latitude and process stability is also presented. Finally this paper discusses about the improvements of this technique to address high resolution and to improve the throughput concerns.

2. CELL PROJECTION CONCEPT

Since several years the electron beam direct write approach based on Gaussian beam or variable shaped beam principle (VSB) has proven its advantages for the realization of advanced devices, prototyping and small volume production [2]. The high resolution capability of these two technologies is widely known. Depending on the type of resists, 20nm resolution can be properly achieved. However the weak point of the electron beam technology remains its throughput capability. Gaussian beam tools are around ten times slower than variable shaped beam approach. Concerning the variable shaped beam technology, table 1 gathers the evolution of the shots number in function of the nodes. Based on a standard writing time of 5 microseconds per shot; i.e. 100µC/cm² resist sensitivity at 50keV accelerating voltage, the writing time per wafer on a VSB tool is also listed in this table. For a 90nm node design, the writing time reaches approximately 0,03wph for 400MB shots number per field whereas it is around 0,007wph for the 45nm node. Ultimately, it is expected to be around 0,005wph for a 32nm product. As described in table 1, the writing time decreases drastically for each new technology node insertion. To get an acceptable writing time of the current electron beam direct write lithography, a new concept of electron beam technology is absolutely needed. The cell projection approach can answer to this need.

nodes	90nm	65nm	45nm	32nm
shots number per field	400MB	900MB	1,8GB	2,5GB
hours/wafer	33	75	150	208
wph	0,03	0,013	0,007	0,005

Table1 : Evolution of the shot number in function of the nodes based on a speed of standard $5e^{-6}$ seconds per shot for VSB

The electron based cell projection lithography is a well known technology developed since several years by Advantest. Figure 1 shows an illustration of the cell projection concept where the first aperture generates an uniform beam and the second aperture finalizes the character formation with a limited maximum size of 4µm*4µm. In a regular variable shaped beam mode the design structures are cut into elementary figures with a maximum shape size of around 2µm. This technology is currently available on the last generation F3000 VSB tool dedicated 45nm nodes technology

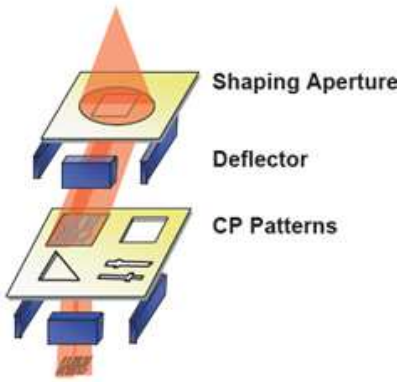


Figure 1 : Illustration of Advantest F3000 cell projection (CP) concept

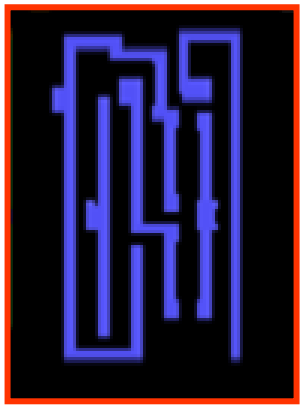


Figure 2 : Example of circuit portion projected by cell projection concept

The complex logic structures can be also exposed as a whole. A bloc of memory cell or a portion of integrated circuit can be effectively projected entirely by the cell projection concept. . The F3000 platform allows also CP projection through a stencil mask. This stencil masks has a total capacity of 1200 cells, but only 100 characters are available per layer. Figure 2 shows an example of integrated circuit portion which can be exposed by cell projection technology in a single bloc in one exposure, comparable to one VSB shot. In VSB mode, this bloc will be exposed in several shots. The advantage of the cell projection technology is therefore the potential shot reduction offered by this approach.

From a courtesy work done previously by Cadence and then supported by its spin-off D2S Inc, the shot account reduction using a cell projection approach based on simple extraction from original design allows to reach a reduction factor of 3 to 5. Figure 3 shows the result of this study on shot reduction from a 45nm design. As mentioned in this mode of cell projection approach, the extraction of the cells is done from an analysis of the GDSII file layout design hierarchy. The reduction factor is then about five by using a potential of a maximum 100 cells per layer. This reduction can be increased to about 25X by introducing the concept of Design For EBeam option (DFEB). Similar to design for manufacturing option used in optical lithography, DFEB readapts the design by including the ebeam lithography limitations (tool, process, character cells size…). New optimised layout is then created for electron beam cells projection lithography. With this DFEB approach the writing time of the variable shaped beam will then become very interesting and attractive as for example the writing time of a 32nm design will be as much as faster than the design of the 90nm nodes.

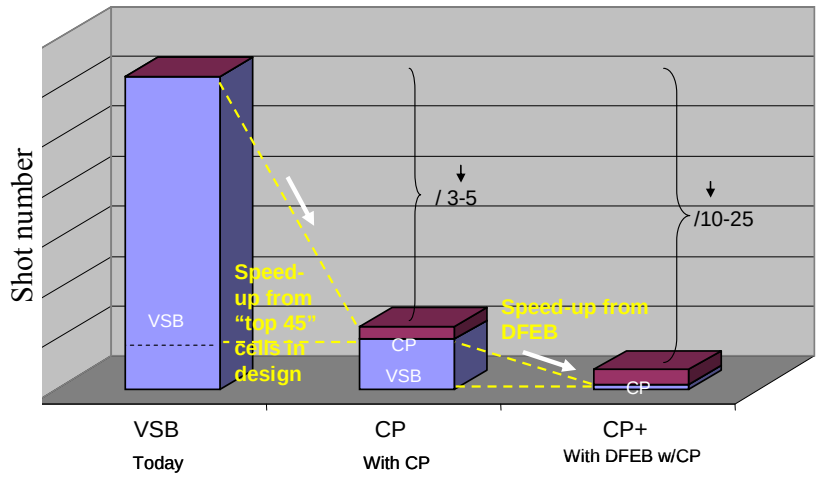
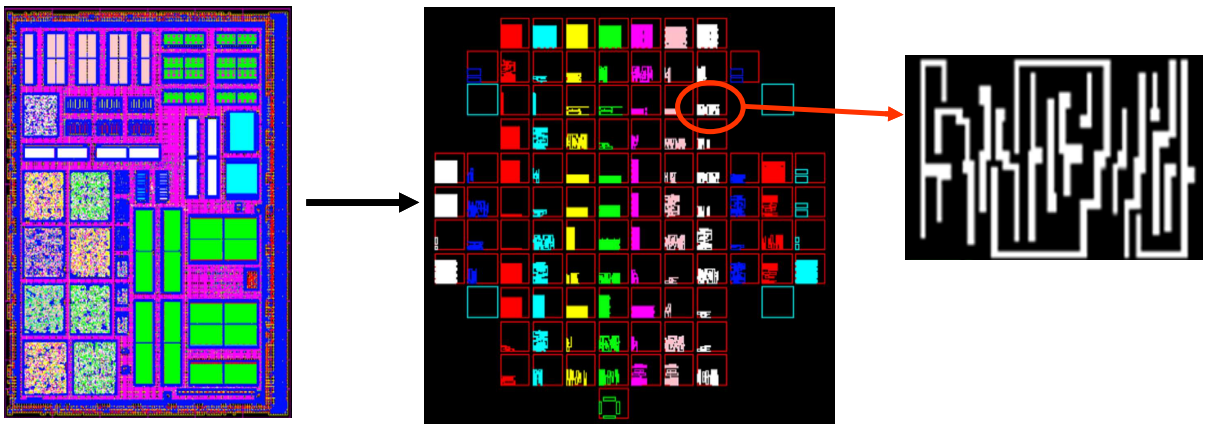


Figure 3 : Shots number reduction perspective using a standard cell projection lithography and an optimised Design For EBeam (DFEB) approach.

3. EXPERIMENTAL CONDITIONS

All electron beam cell projection lithography experiments were performed with Advantest last generation single shaped beam F3000 tool handling 300mm wafer size. This tool works with a LaB6 electron source at an acceleration voltage of 50keV and a current density of 20A/cm². The resists used to coat silicon wafers were positive and negative chemically amplified resists with a thickness of 150nm. All original 65nm, 45nm and 32nm design layouts have been provided by STMicroelectronics. These designs have been first analysed by D2S for cells identification and extraction. Figure 4 shows an example of the 65nm PROMO memory design layout analysed and from which the most repetitive CP cells have been extracted (figure 4b). Principle of the cells extraction is simply based on an analysis of the GDSII file hierarchy and a research of the repeated cells. As at the number of cells extraction is presently limited to 100 cells per layer on Advantest tool, a manual analysis of the extraction result is then performed to finalize the choice of the final CP cells. Thereafter a stencil is been then manufactured including the most repeated cells. Advantest applied then the necessary proximity effects correction and generated the right format for exposure.



a b

Figure 4: Cells extraction from 65nm memory cells GDSII file (a) and cells placement on stencil mask (b)

4. RESULTS AND DISCUSSION

4.1 Cell Projection patterning

Experimental patterning results obtained with cell projection principle are in general good and comparable to ones obtained by using standard variable shaped beam strategy. Figure 5-a shows a portion of the 65nm PROMO design patterned with and without CP. No difference can be observed between CP and VSB modes. The CP cells are filled and the VSB shots are not filled. The colour indicates the exposure dose applied to each CP cell or to each VSB shot. The experimental result of this portion is shown in figure 5-b. First results show that 65nm line width can be achieved with both VSB and CP approaches. However several discrepancies have been shown in CD uniformity using CP compared to the full VSB techniques. The CD uniformity error goes up to 10nm using the CP techniques. For the 65nm line widths, this error can be recovered by a more robust dose assignment [5].

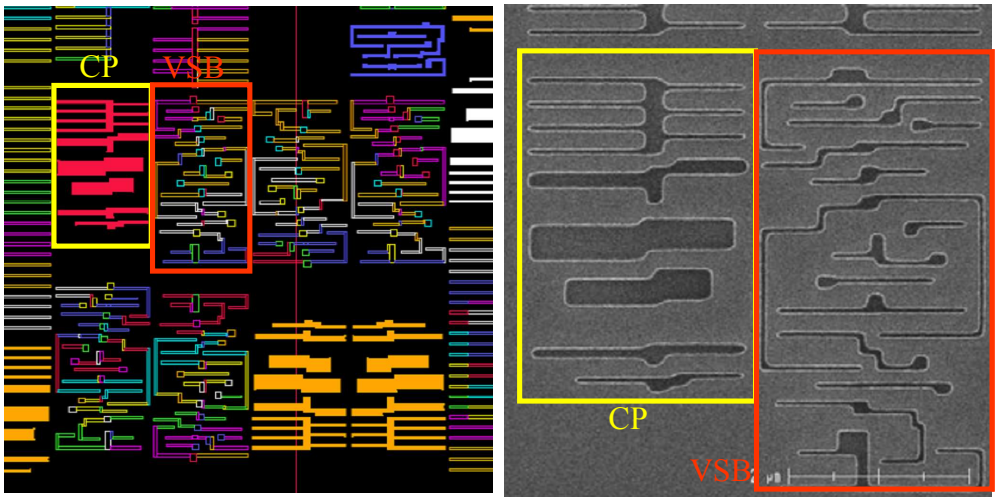


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Figure 5 : Example of a data base having the CP and VSB shots (a) and the results on wafer (65nm line width) (b)

For the sub 65nm nodes, the CD uniformity error increases whereas the line width decreases. There are two types of CD uniformity errors. The first one is linked to the cell itself and the second one concerns the CD uniformity between cells patterned in VSB or in CP modes. In both cases, the matching of the linewidth cannot be done with the current dose modulation correction only. The dose modulation widely used in VSB lithography to correct the proximity effect. However, in this case, the CD uniformity is limited in the cell projection technique as dose cannot of course be adjusted directly inside the cells. Therefore a complementary geometrical based on shape correction approach [6] may recover this limitation of the current dose modulation approach.

Figure 6 shows a comparison result of the 65nm SRAM structures obtained without (figure 6-a) and with (figure 6-b) shape correction approach. In each case, results obtained with variable shaped beam technique is compared to the result obtained using the CP approach with and without the geometrical approach. Using a design correction approach in the cell offers a higher flexibility not only for the CD uniformity errors but also in general proximity effects correction as for the correction of the line end shortening, corner rounding...

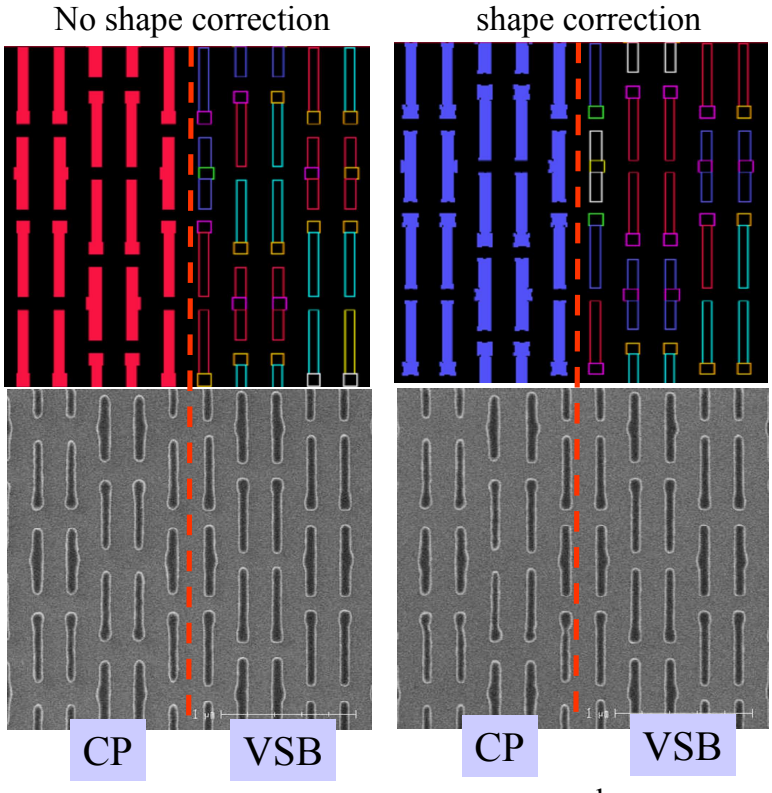

Figure 6 : Comparison of the 65nm SRAM structures obtained without (a) and with shape correction (b)

Nevertheless, the use of geometrical correction VSB+CP lithography has to be tightly controlled especially for the high-resolution patterning as this will turn out in a use of very complex proximity effects models which can impact deeply the data preparation cycle time. On one side getting a gain in the EBDW writing time can induce a loss in the other side through the data preparation cycle time due to this complex model preparation. A compromise needs to be found in the use of design correction in cell projection lithography. One of the solutions could be the use of very simple geometrical approach combined with a smart CP cells choice in order to simplify the deployment of the proximity effects corrections. Figure 7 shows an example of the 45nm SRAM structures patterned at 44nm line width with a 120nm

pitch. In CP cells area, shown in yellow in figure 7-a, several VSB shots are exposed between structures printed in CP mode. In this case, CP cell structures have more flexibility to be corrected in term of geometrical or dose correction. Figure 7-b shows good results on wafer with a better control of CD uniformity. However in our example, some improvements are still needed on the line end shortening control as some bridging effects can be oberved in the line ends area.

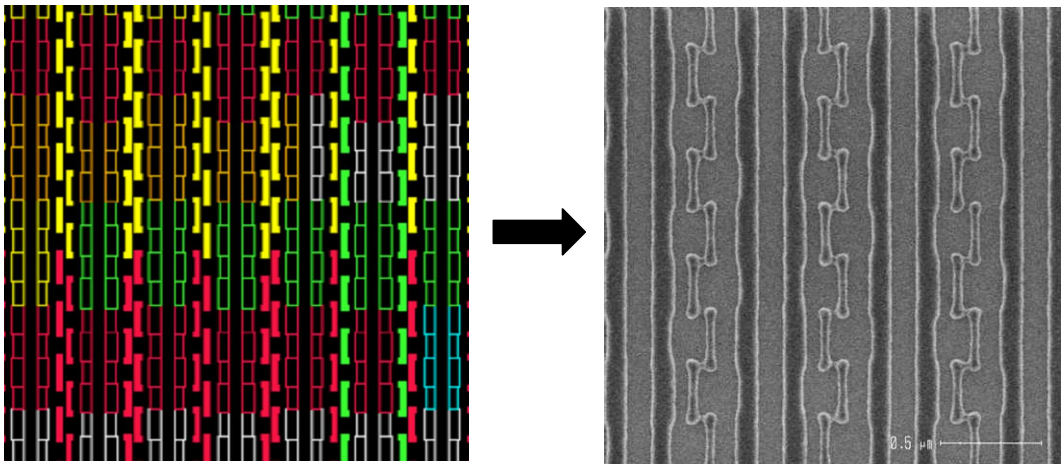

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Figure 7 : 45nm SRAM structures active level patterned at 44nm line width with a 85nm pitch

The insertion of the cell projection technique in a manufacturing use can not be done without a good placement of the CP cells on wafer. Table 2 gathers the stitching data regarding the CP cells versus VSB shots average. This stitching tests show that the average stitching of CP cell compared to the VSB shots is less than 4nm. This result is good enough for the 45nm nodes patterning and needs to be improved for the 32nm nodes patterning. These stitching results are in respect of the F3000 tool specifications as this tool is defined to answer the 65 and 45nm nodes.

	X	Y
Mean	-0.1nm	0.4nm
3sigma	2.6nm	3.2nm
total	2.7nm	3.6nm

Table2 : CP cells versus VSB shots average stitching results using the Advantest F3000 tool

4.2 Cell Projection resolution capability for contact and via levels

With the cell projection technology 40nm contact-hole structures can be achieved with a good CD control. Figure 8 shows the results of 32nm node contact-hole structures drawn at 40nm and patterned at about 40nm on wafer with the cell projection technique. Contact hole are well defined on the wafer whereas the shared contact structures with a dimension of 40nm*100nm need some improvements in terms of CD size and line end shortening. These discrepancies can be easily compensated with a simple shape correction. Figure 8-b shows the corrected result of the 40nm SRAM contact level obtained with cell projection including a

shaped CP correction. Shared contact width is then reduced to the right CD of 45nm and the line end shortening is corrected to a 2nm loss per edge.

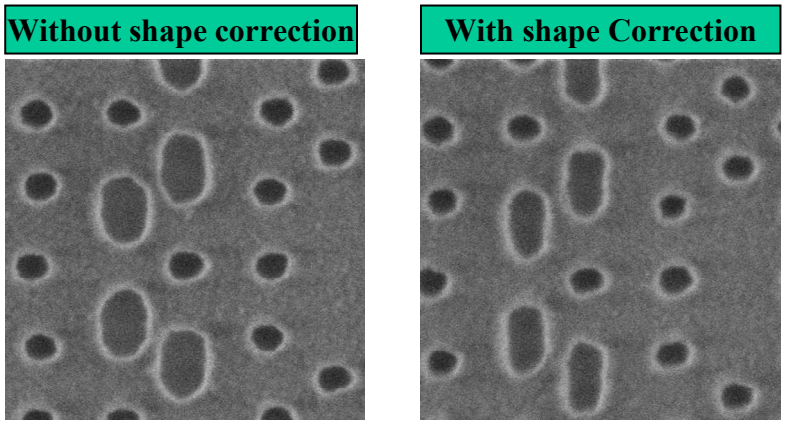

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Figure 8 : 32nm contact hole structures patterned at 40nm without (a) and with (b) shape correction

4.3 Throughput gain

The introducing of cell projection technique in the electron beam variable shaped beam should lead theoretically to a global shot number reduction. This is experimentally verified and presented in the graph below. A comparison of the shot number of a 65nm contact level layout (SRAM memory PROMO product) fractured with a full variable shaped beam and with cell projection option is detailed in figure 9. The same comparison has been also done for the 45nm contact level (figure 10) where the PROMO product is also fractured with the both options. In each cases, a shot account reduction of a factor around 6 is obtained with the CP technique. Therefore the first step in terms of shot count reduction perspective as presented in figure 3 is already demonstrated.

This shot count reduction is of course deeply dependant of the cells size. The larger cells size is, the better will be the shot number reduction. Unfortunately the limitation of the CP cell size is mandatory as larger cells size increases Coulombian interaction and so a loss in resolution. In this experience, we used a maximum CP cell size of 4x4µm².

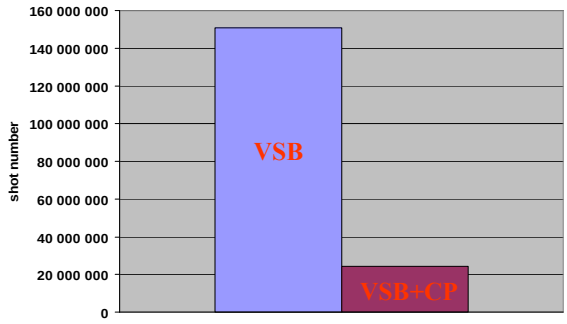

Figure 9 : Shot reduction obtained with Cell projection applied to the 65nm PROMO contact level

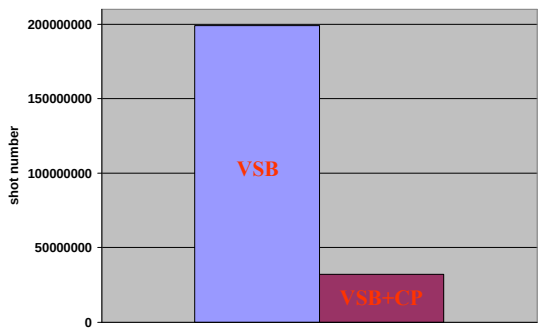

Figure 10 : Shot reduction obtained with cell projection applied to the 45nm PROMO contact level

5. CONCLUSION

The electron beam cell projection technology is presented as an extension of the variable shaped beam lithography. A detail description of the CP concept with its possible technology limitations for sub 45nm nodes is described in this paper. In general, good patterning results have been achieved using this technique. However a complementary geometrical correction solution is needed to recover the standard dose modulation approach used for the electron beam proximity effects corrections.
The main advantage in the use of the cell projection remains in its throughput gain where a shot reduction of about 5 can be achieved compared to the variable shaped beam lithography. Next step will be the optimisation of EBDW writing time using cell projection lithography with the design for the ebeam (DFEB) option.

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REFERENCES

1. L. Pain et al., Proc. SPIE, vol. 5037, 560-571, (2003)
2. L. Pain et al., Proc. SPIE, vol. 5751, 35-45, (2005)
3. H.C. Pfeiffer, IEEE Trans. Electron.Devices ED-25(1979) 633
4. O.K. Fortagne et al., Microelec. Eng. 27, 151-154, (1995)
5. S. Manakli et al. Jpn. J. Appl. Phys. 45 (2006) pp. 6462-6467
6. S. Manakli et al. J. Micro/Nanolith. MEMS MOEMS Vol.6 (3), Jul-Sept 2007