



Mask patterning challenges for EUV N7 and beyond

Date: 2018/02/27

Outline

- ▶ **EUV tech drivers and mask roadmap**
- ▶ **N7 mask process status**
- ▶ **Mask and mask process characterization**
- ▶ **Process improvements toward N5**

EUV technology drivers

Type	2017	2018	2019	2020
Logic	10nm	7nm	5nm	
DRAM	1x	1y	1z + new architectures	
3D NAND	Gen 2	Gen 3	Gen 4 + new architectures	

► Roadmap drives scanner and subsequent mask improvements

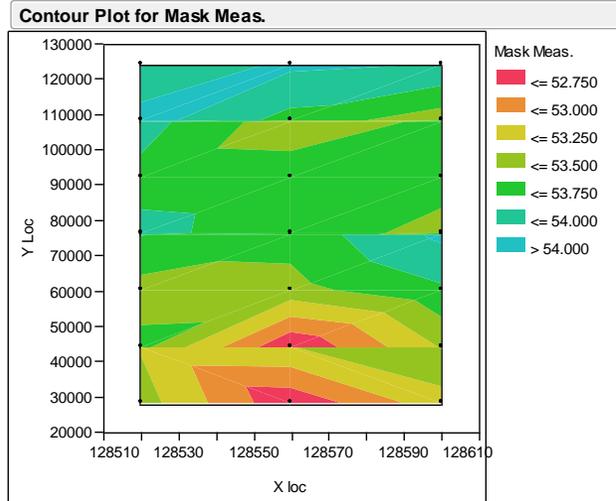
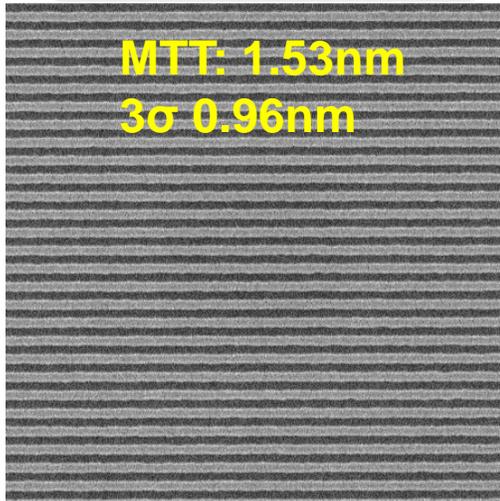
- Minimum feature resolution-main & SRAF
- Pattern fidelity & LER
- CD control-MTT, CDU, linearity, etc
- Pattern placement
- 3D effects
- Black border (including OOB suppression)

EUV Mask capability roadmap

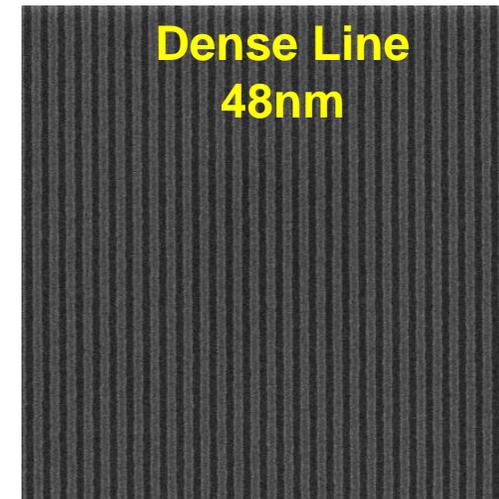
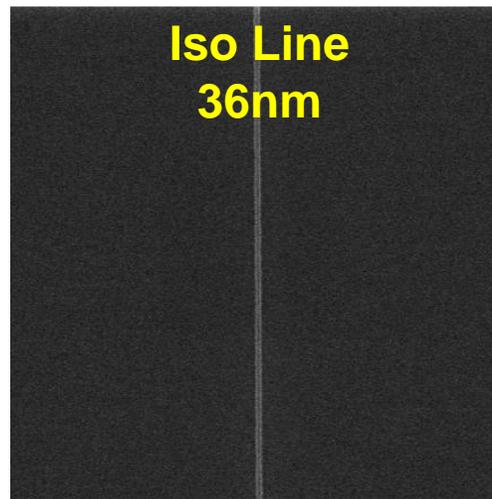
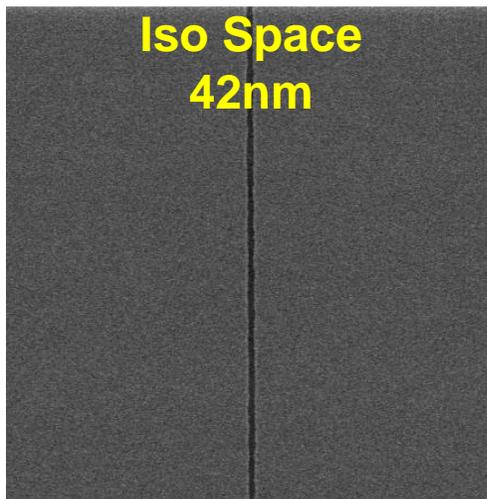
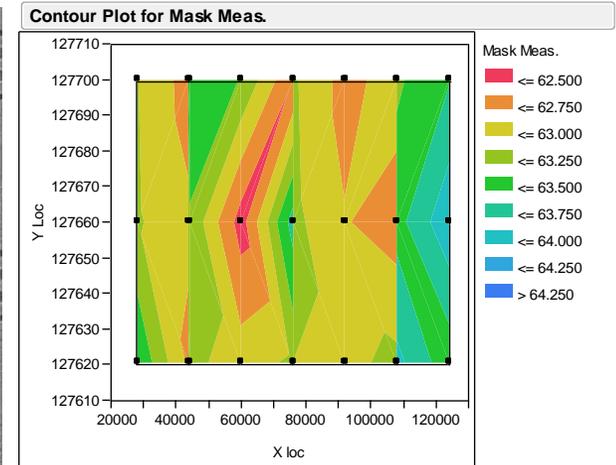
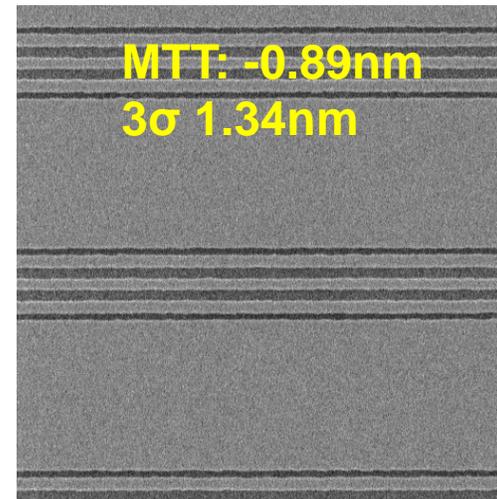
Attribute	Target for mask readiness		
	EUV N7	N5	N3
	2017	2018	2019 & beyond
Main CD (nm)	52	44	30
SRAF (nm)	40	30	24
CD Uniformity (3 σ , nm) Spec/LS Capability	3.0/1.5	2.5/1.3	2.0/1.1
Registration(3 σ , nm)	3.0	2.0	1.5
Linearity (nm) (50nm – 500nm; IL, IS DL)	≤ 5	≤ 4	≤ 3
Roughness: LER/LWR (3 σ , nm)	≤ 3.0	2.5	2.0
3D Effects-Blank Materials	<ul style="list-style-type: none"> • Ta-based Abs. • 60nm Thick 	<ul style="list-style-type: none"> • Ta-based Abs. • 55nm Thick 	<ul style="list-style-type: none"> • Alternate Abs. material • 30-35nm to support high NA
Black Border	$\leq 0.05\%$ reflectivity (λ from 12.80 - 14.2nm) $< 2\%$ Out of band reflectivity (λ from 100 - 280nm)		

N7 process performance

52nm Dense Line

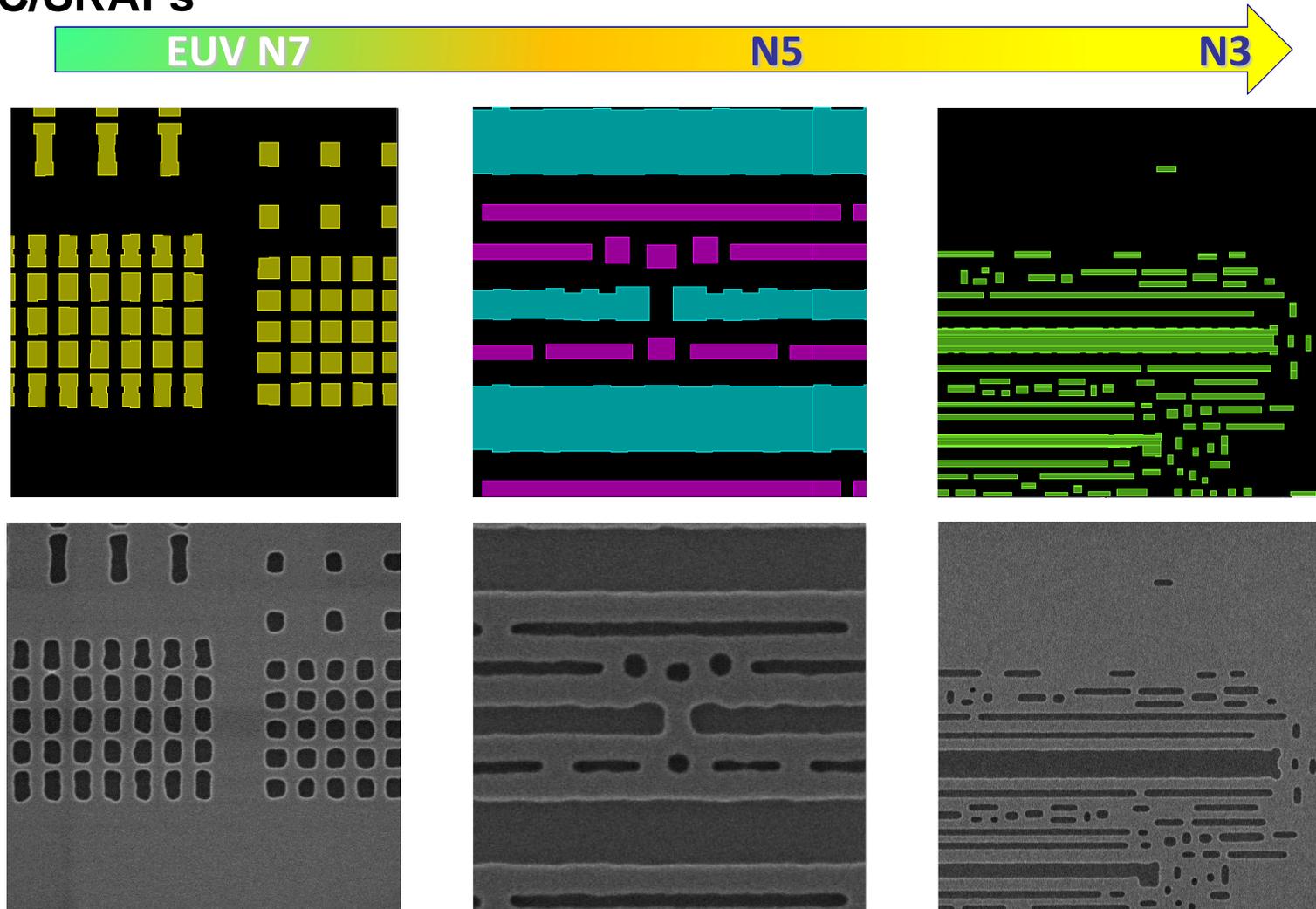


64nm Space/40nm SRAF



Challenge: increasing pattern complexity

- ▶ 2D structures are critical at N7 and increase in complexity through N5 with increasingly aggressive OPC/SRAFs



Characterizing pattern fidelity

▶ Edge roughness & other mask process-induced error

Low frequency LER on mask - high impact on wafer
 → Mask LCDU is critical

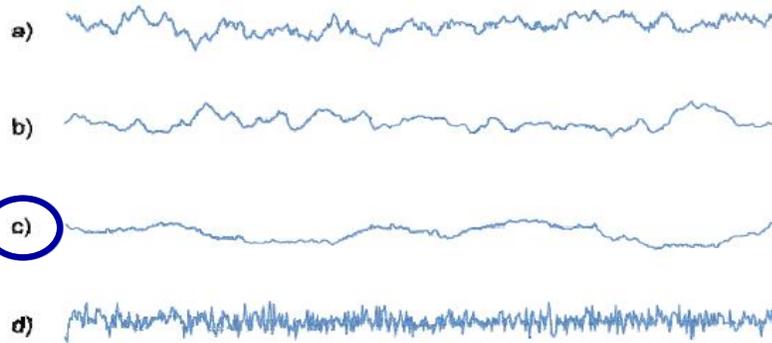
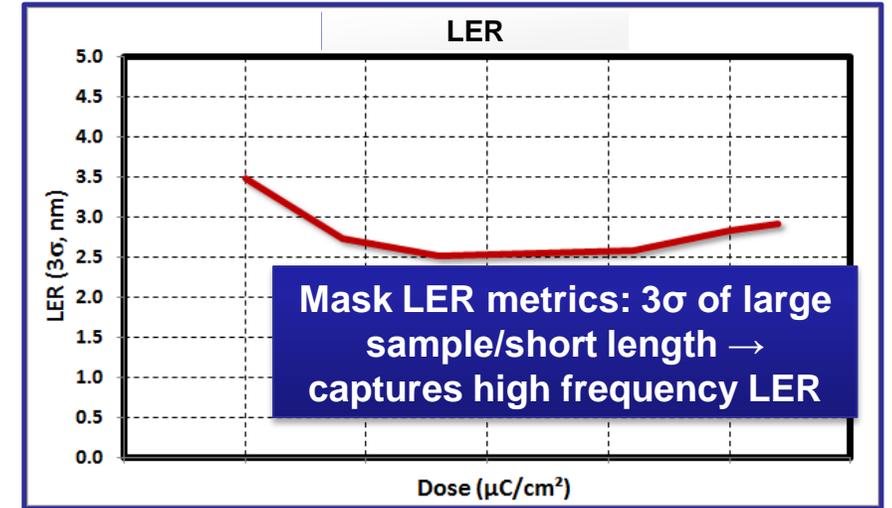
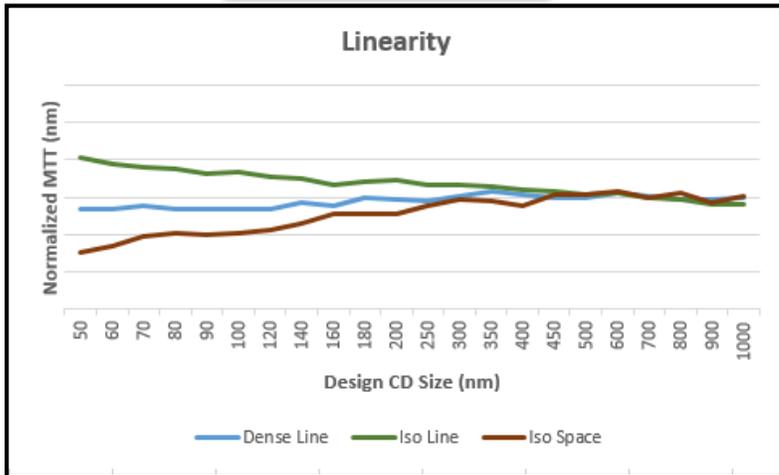


Figure 1. These four randomly rough edges all have the same standard deviation of roughness, but differ in the frequency parameters of correlation length (ξ) and roughness exponent (H): a) $\xi = 10$, $H = 0.5$, b) $\xi = 10$, $H = 1.0$, c) $\xi = 100$, $H = 0.5$, d) $\xi = 0.1$, $H = 0.5$.

[C. Mack, Proc. of SPIE Vol. 10450 104500P-2]

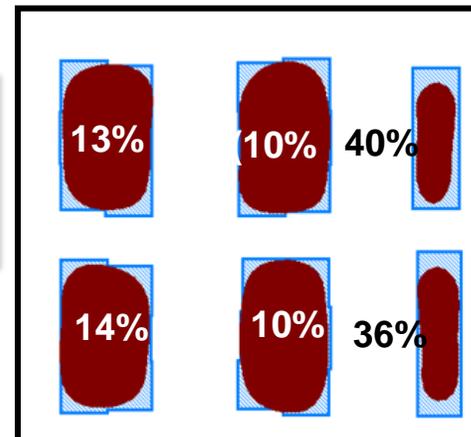


1D Metrics



Mask Process Error Characterization

2D Metrics - mask contour

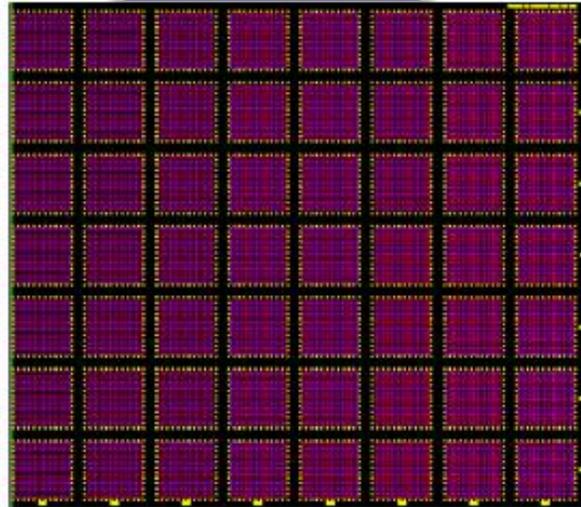


Area loss vs design or other EPE metrics

Mask process development and mask process error correction

Defining process capability

Device-like test chip w/ aggressive OPC features



- Bias

0 Bias

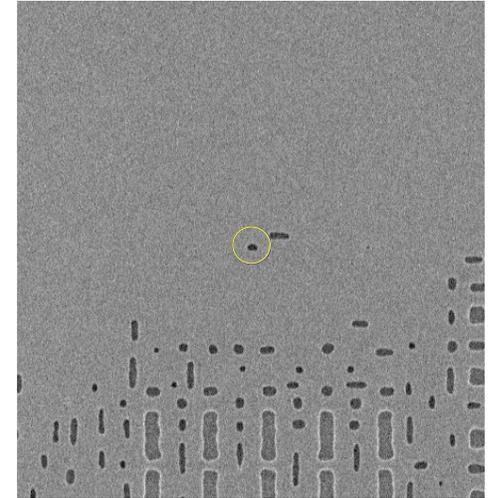
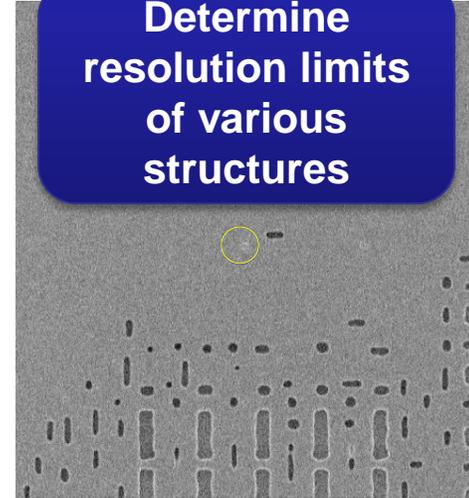
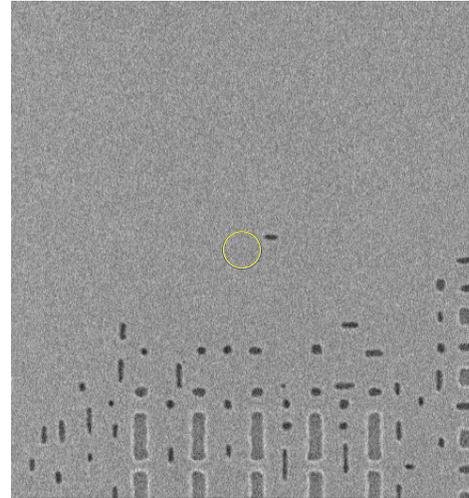
+ Bias

Smallest

Pitch Scale

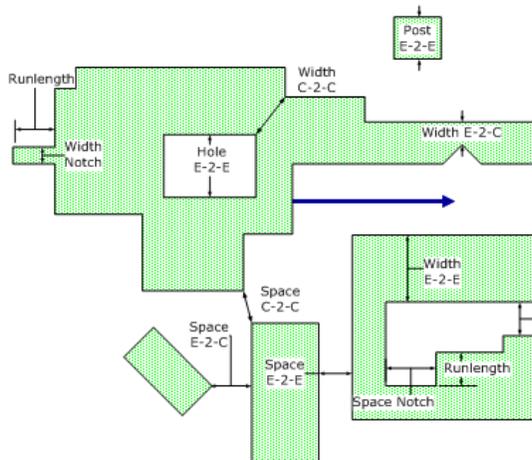
Largest

Associate geometries with MRC Rules



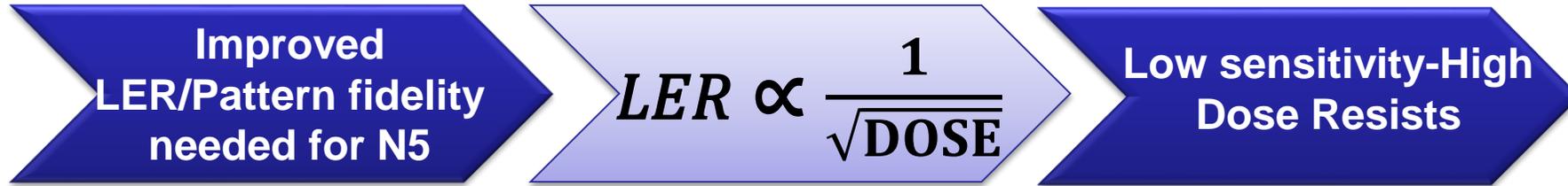
Determine resolution limits of various structures

Clear Shrink

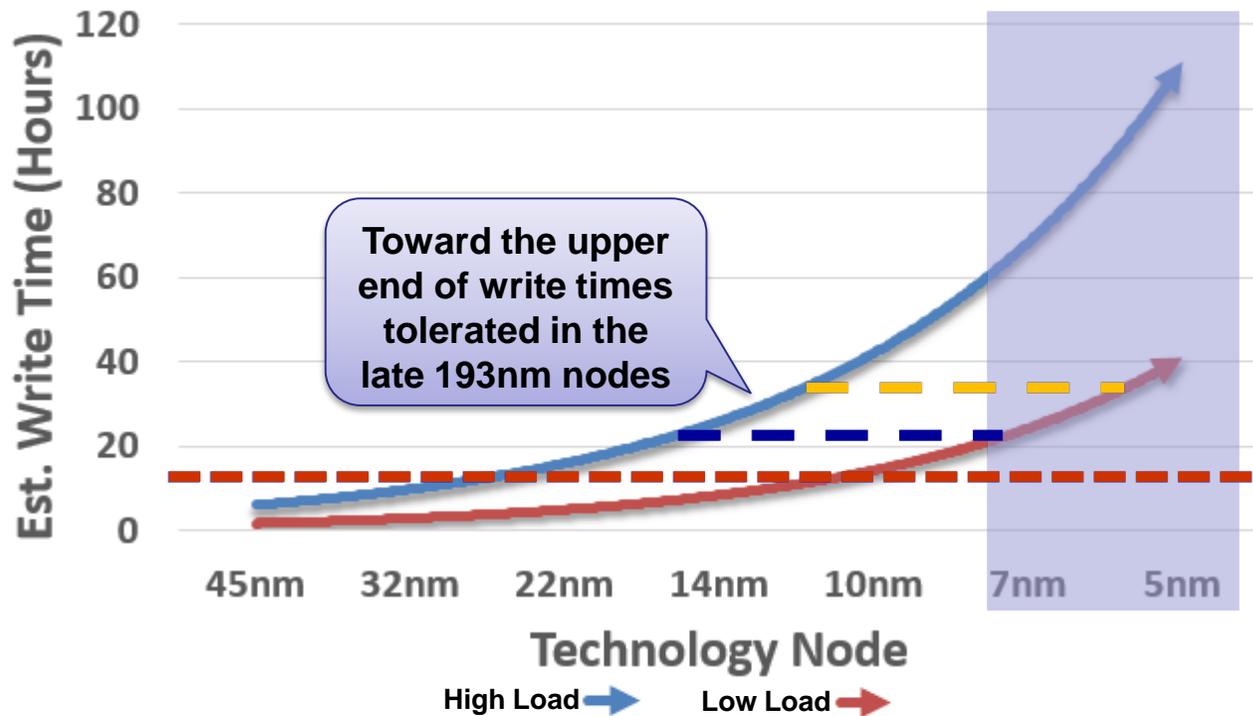


Rule
Min Width Edge-2-Edge
Min Width Edge-2-Corner
Min Width Corner-2-Corner
Min Notch Width (runlength)
Min Post Width Edge-2-Edge
Max Post Aspect Ratio
Min Space Edge-2-Edge
Min Space Edge-2-Corner
Min Space Corner-2-Corner
Min Notch Width (runlength)
Min Hole Edge-2-Edge
Max Hole Aspect Ratio

Improving pattern fidelity



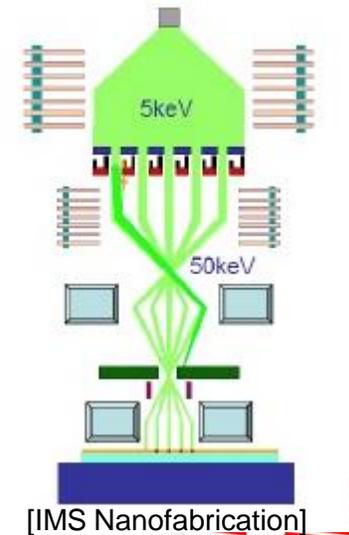
Estimated VSB Write time



High dose CARs or chain scission type resists 60-150 $\mu\text{C}/\text{cm}^2$

>4pass VSB writing feasible for some applications - low load or small field test masks

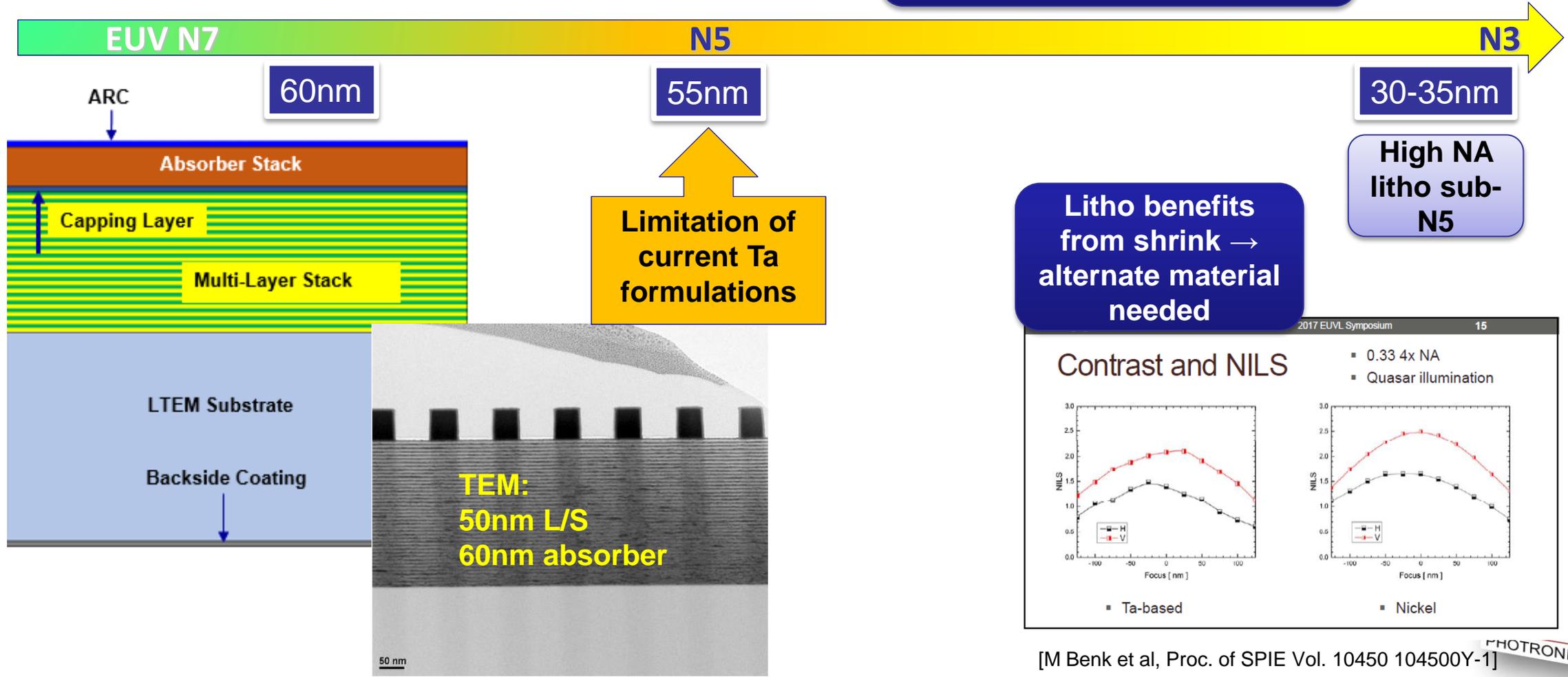
Ultimate solution for N5 HVM: MBMW



Optimizing the blank material

Minimize M3D effects → shrink the absorber stack

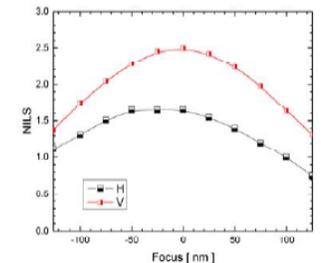
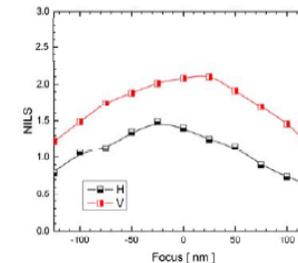
Faster etching, thinner films → enable thinner resist → improved minimum resolution



Litho benefits from shrink → alternate material needed

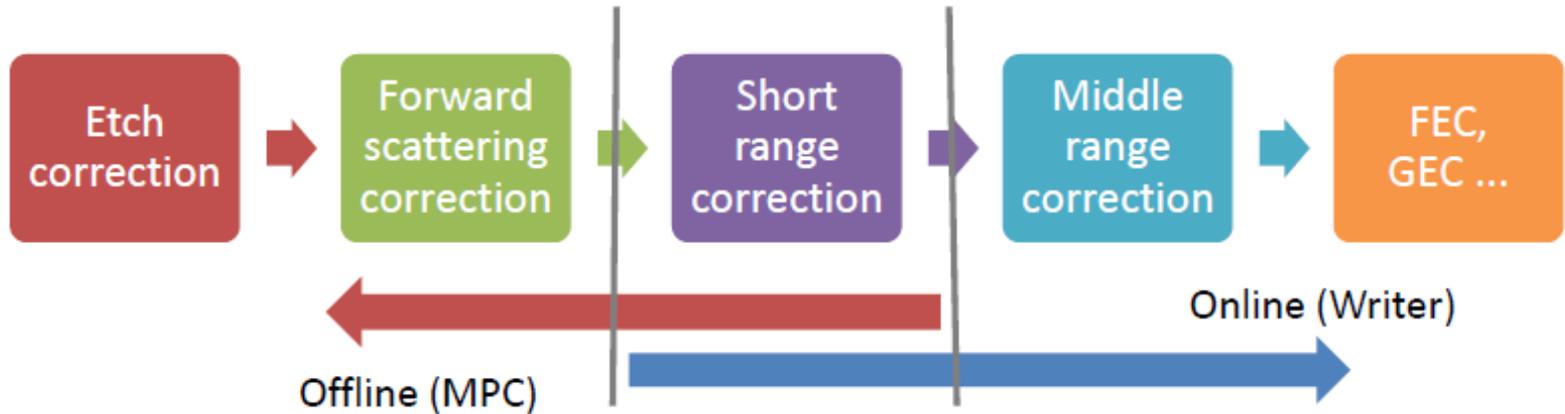
High NA litho sub-N5

Contrast and NILS

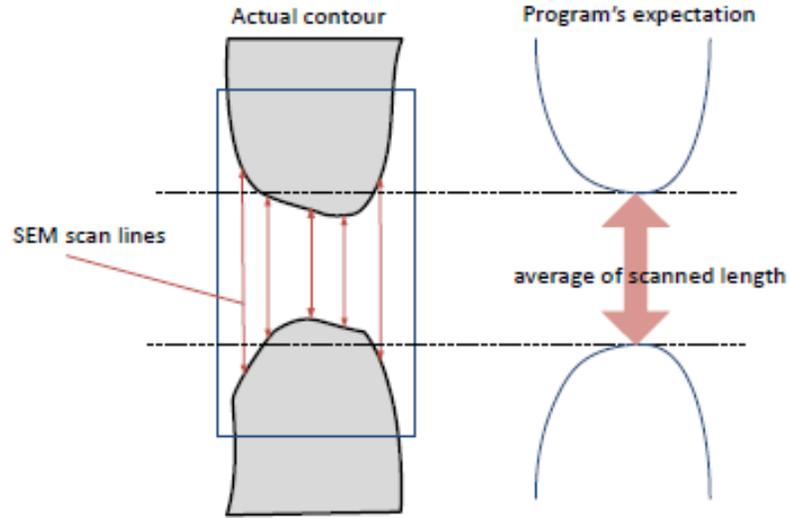


Data solutions-MPC

Account for inherently different proximity effect in EUV blanks-short range backscatter



Account for 2D structures using actual mask contours for model building



We use contour images for 2D because using the measured CD may not duplicate the actual CD at line ends.

Provide more accurate MPC models

- Additional component to capture local/proximity effect
- Decouple the effects which should not be considered in model
- VSB/MBMW specific effect



Pattern placement

N7 Class EUV Mask

Solutions toward N5 & beyond

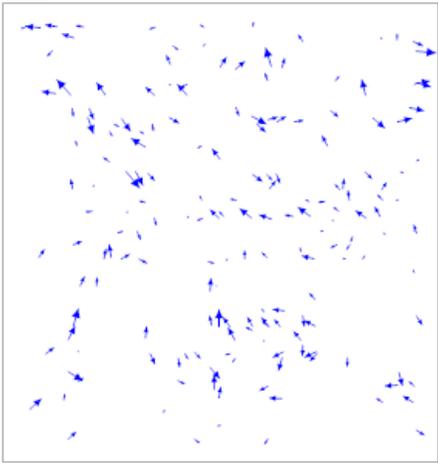


In die metrology for larger sample size and accurate custom writing grids

Physical charging countermeasures → charge dissipation layers (CDLs)

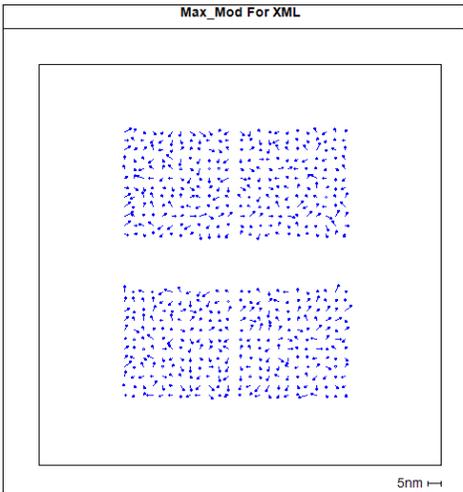
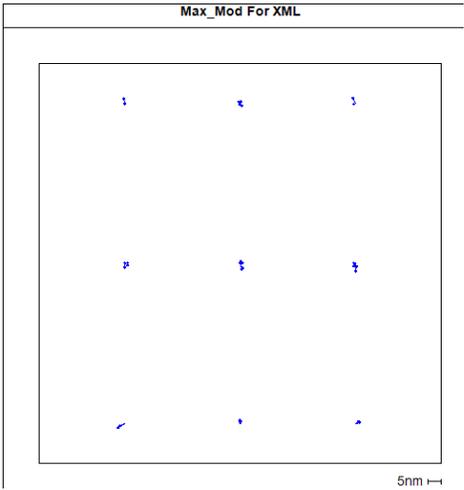
Improved computational methods for charging effect correction

Advanced writing platforms



0.005 [μm]

	X (nm)	Y (nm)
Max 3σ	2.95	2.91
Min	-2.09	-2.24
Max	2.80	2.52



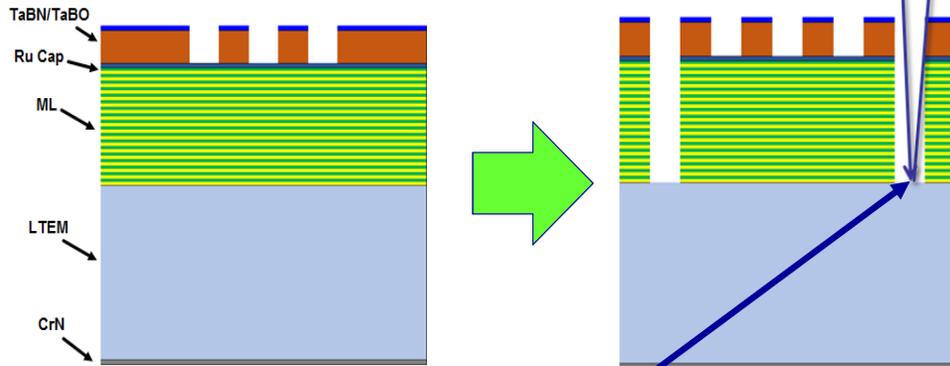
Black Border

- ▶ Need OOB suppression from 100nm - 280nm target <2% average reflectivity
- ▶ Photonics proprietary process

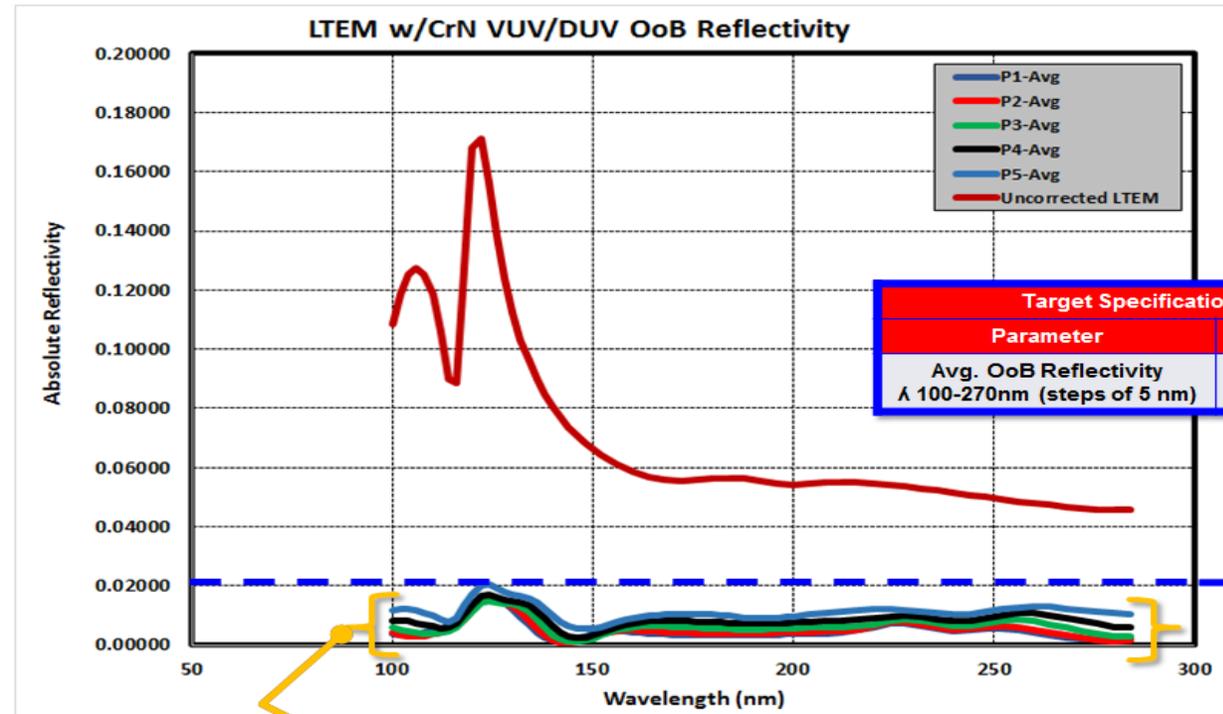
OOB Reflectivity after Photonics
BB Process
(measure at PTB, Germany)

VUV/DUV Reflectivity: ???

EUV Reflectivity: $\leq 0.10\%$



High OOB reflectivity on untreated LTEM surface

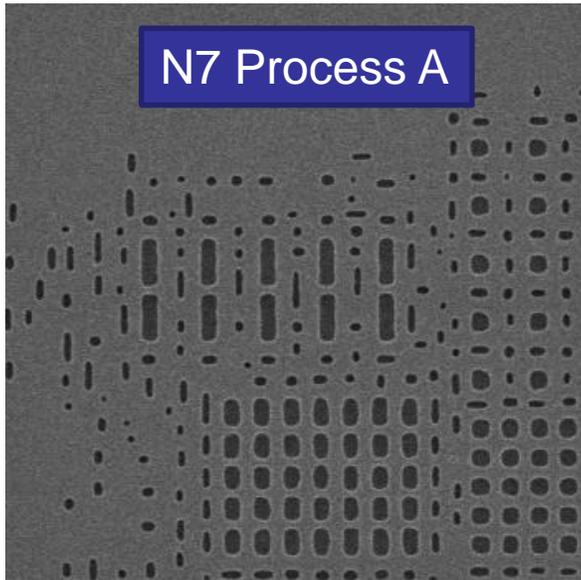


Target Specifications	
Parameter	Specification
Avg. OoB Reflectivity λ 100-270nm (steps of 5 nm)	$\leq 2.0\%$

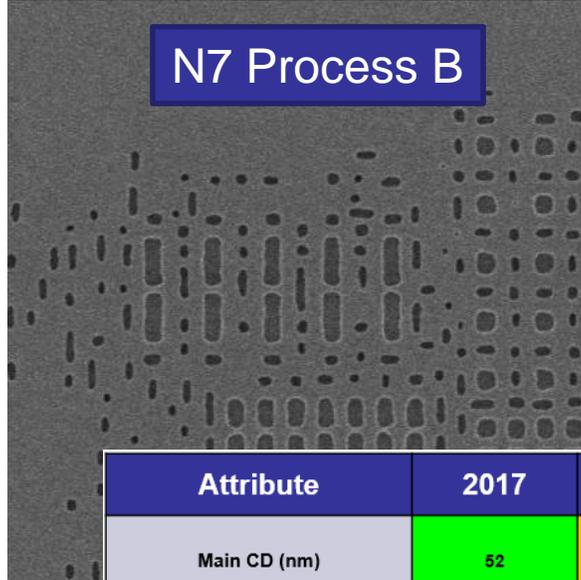
Process window well within OoB suppression requirements

Putting it all together

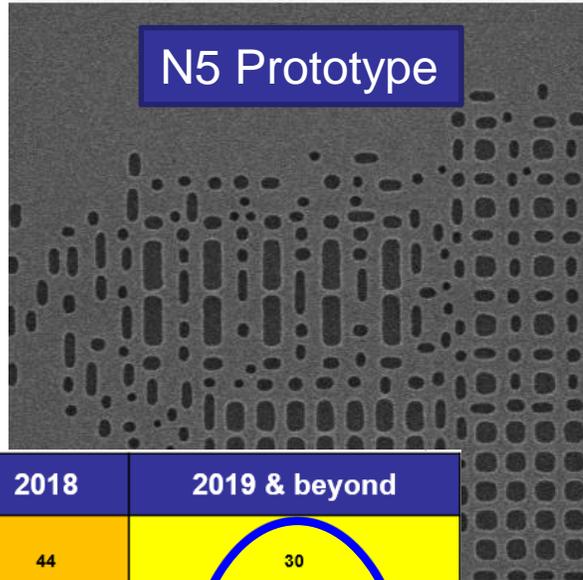
Iterative process development toward N5



N7 Process A



N7 Process B



N5 Prototype

Target mask capability to support N5 and early N3 R&D within next 2 years

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Summary

- ▶ **Processes for EUV N7 are known and in place across the industry**
- ▶ **N5 and beyond presents new mask patterning challenges**
 - Increased pattern complexity with proliferation of SRAFs
 - Escalating error contribution of mask 3D effects
- ▶ **Solutions moving forward**
 - Enhanced mask characterization
 - Lower sensitivity resists
 - Mask data manipulation for mask process error correction
 - Blank material innovations