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Lithography alternatives: Why are they essential?

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The availability of patterning alternatives in the lithography landscape represents a big opportunity to properly address the coming needs generated by the IoT.

The Internet of Things (IoT) is expected to fuel significant growth opportunities for the semiconductor industry, as demand increases for wireless components and more and more embedded functionalities such as memory and sensors. This growth will affect almost all integrated circuit (IC) sectors (**FIGURE 1**). The chip industry will continue to need advanced technologies to provide the most powerful functionalized ICs with lower power consumption for the IoT, but manufacturing costs remain a key challenge. Lithography and related patterning technologies can represent up to 50 percent of total IC production costs, and significant efforts have to be made in the coming years to slow and even reverse this trend.

In the lithography landscape for the development of advanced technology nodes, extreme-UV (EUV) lithography technology recovered some credibility at the beginning of 2015 with the release and installation of the first 80W power sources[1]. However, its adoption by the industry remains uncertain, because its infrastructure still requires significant development. Also, the recurrent questions about the real cost of ownership associated with the ability of the 0.33NA platform to address sub-7nm technology nodes continue to dominate the debate in the semiconductor community, especially since 3D-stacking strategies are being seriously investigated. This potentially could slow demand for high-resolution and therefore delay the new advanced lithography solutions.

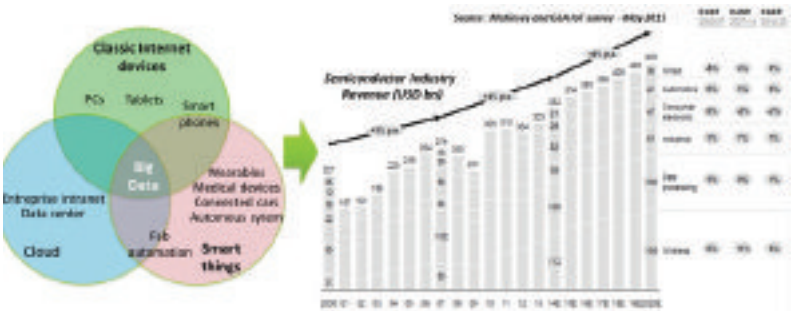

FIGURE 1. Impact of the IoT on semiconductor industry revenue from 2000 to 2020.

Meanwhile, 193nm immersion lithography, with double- or quadruple-patterning strategies, supports the industry preference for advanced-node developments, despite the tremendous effort required for process controls (alignment, mask manufacturing etc.). In this landscape, lithography alternatives maintain promise for continued R&D because they may present competitive compromises for the industry. Massively parallel electron-beam and nano-imprint lithography techniques remain highly attractive, as they can provide noteworthy cost-of-ownership benefits for IC manufacturers. In addition, directed self-assembly (DSA) lithography with block copolymer shows promising resolution capabilities and appears to be an option to reduce multi-patterning strategies, and therefore the associated mask-set budgets. But what is the current status of these technologies? Are they really able to meet

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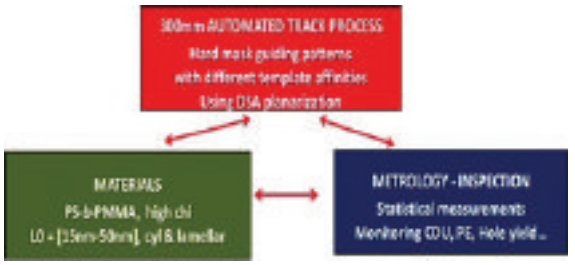

FIGURE 2. CEA-Leti schematic on DSA process environment validation

industry expectations for advanced technology nodes? Are they indeed able to reduce manufacturing costs? What are their introduction points into the production environment?

CEA-Leti is working to answer these questions and has initiated collaborative R&D programs to assess and boost the development of these alternative technologies through strategic partnerships. Three programs have been launched with the primary goals of demonstrating that these lithography options can meet industry needs, assessing industrial use of them and proposing to Leti's IDM partners real turn-key integrated process-flow solutions.

- **IMAGINE:** launched in 2009 with MAPPER Lithography, this program is pushing for the insertion of massively parallel direct-write electron-beam technology. Other participants include TSMC, STMicroelectronics, Nissan Chemical, Mentor Graphics, SCREEN, Tokyo Electron and Aselta Nanographics.
- **IDEAL:** DSA lithography represents a promising solution for advanced patterning. Leti has worked with Arkema since 2011 on the qualification and demonstration of materials for insertion into industrial production flow. Other partners include ST, Tokyo Electron, SCREEN, Mentor Graphics and CNRS-LCPO.
- **INSPIRE:** established in 2015 with the EV Group, this program will focus on the assessment of imprint technology on large-scale patterning.

Directed self assembly: the resolution is in polymer matrix

Since 2010, DSA has steadily attracted attention of R&D laboratories and the IDM industry. The natural high-resolution capability of the block copolymer (sub-10nm) may meet the requirements of future technology nodes. Significant work in this area is underway at R&D consortia such as imec, IBM Research in Albany, N.Y., and Leti, as well as directly in the fab[2,3]. For example, Leti and its partners put in place a full infrastructure to qualify the new material developed by the chemical company Arkema (**FIGURE 2**). A full 300mm line is operational at Leti using a Tokyo Electron track and a customized SCREEN DUO track able to handle the latest process possibilities. This type of infrastructure is required to validate in fab-like conditions the new materials (PS-PMMA and high chi platforms) and their associated integration flows. Those operating conditions give industry the capability to quickly evaluate the full process-flow performances with all the required classic statistical data for final validation.

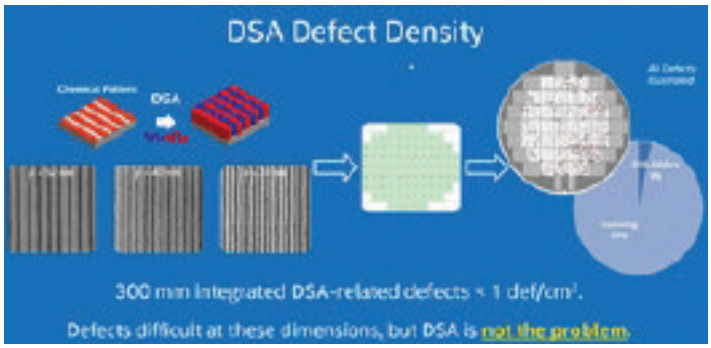

FIGURE 3. DSA defectivity trend on lamellar. Courtesy T Younkins (Intel) - Private communication.

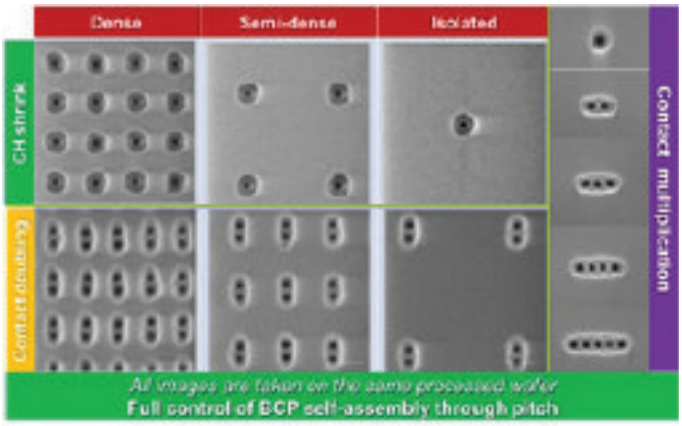

FIGURE 4. Control of iso-dense bias density in Leti DSA

	Not optimized surface affinity control	Optimized surface affinity control
Hole Open Yield	93%	100%
CDU_{DSA} (3σ)	20 %	4,9 %
Placement Error	1,5 nm	0,9 nm
CDU_{DSA} mapping		

FIGURE 5. Influence of surface affinity on key manufacturing-process parameters

Focusing on defectivity Intel showed convincing data at 1def/cm² on line-and-space structures, confirming the potential of DSA to reach the ITRS target and therefore to be used for manufacturing in the near future (**FIGURE 3**). As well, Leti results on grapho-epitaxy process are also very encouraging with zero visual-defect process flow for contact/via application measured with low statistical level[4]. Those results are the first positive key trends in the DSA technology. Evaluating the compatibility of DSA with semiconductor process flows is the next important step. The control of the iso-dense configuration focused

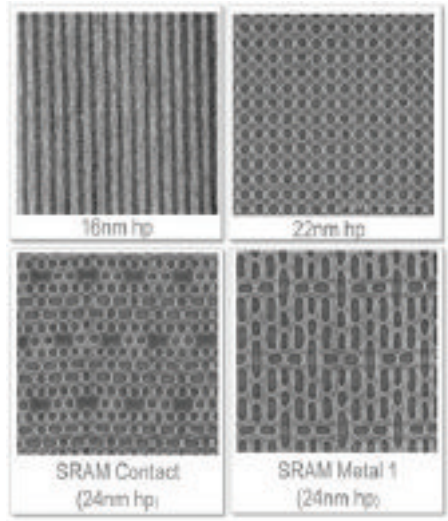

FIGURE 6. Example of MAPPER Lithography patterning capability on the pre-alpha platform[5]

a lot of attention on the grapho-epitaxy process, in which block copolymer film-filling uniformity is affected by the topography effects of the guide patterns. Leti developed and patented a flow allowing a proper control of CD and CDU in all density configurations. (**FIGURE 4**) This solution preserves the interest of DSA as it is integrated in the process flow itself and because it does not imply a need for any additional design-rule restriction[4].

Nevertheless, some hurdles remain to be overcome before its final adoption. The control of the surface affinity is one key aspect. It can greatly affect the final defectivity level and impact the complexity of the integration flow (**FIGURE 5**). Any non-uniform control of the bottom residual polymer thickness in the bottom of the guide cavity may lead to post-etch opening issues and final circuit-yield drop. Moreover, to be fully adopted, DSA technology also must be aligned with the compatible design rule manuals. Insertion in the DRM is essential and it implies adding new specific constraints due to the nature of the block copolymer and to the lithography guide realization. All these R&D efforts must be pushed to value the advantages of DSA technology: the natural high resolution of this solution and its cost effectiveness from reducing multi-exposure strategy. In addition to ensuring DSA's ability to extend 193nm immersion lithography, it also supports the use of the EUV 0.33NA tool for the development of 7nm nodes and below.

Massively parallel electron-beam writing

Despite recurrent delays in new developments, parallel electron-beam lithography remains an attractive alternative option. The massively parallel writing solutions developed by MAPPER Lithography and IMS Nanofabrication for wafer and mask writing, respectively, offer good compromises: a significant alliance of resolution and

advantageous manufacturing costs. But this technology also benefits from additional advantages, such as writing flexibility and a significant throughput improvement due to the parallel exposure concept that can boost the throughput in the future up to 100 wafers per hour in a cluster-tool configuration. First pre-industrial units are today installed in pilot-line environments, foreshadowing their introduction into production lines in coming years.

MAPPER and Leti's collaboration is focused on introducing this technology for direct-write application. This joint program started in 2009 around the MAPPER's pre-alpha tool that validated the key concept of the MAPPER technology in terms of parallel writing and resolution capabilities (**FIGURE 6**). The partnership entered in a new phase in 2014 with the installation of the first FLX-1200 pre-production platform, (**FIGURE 7**), operating 1,300 beam lines for a targeted throughput of 1 wph and then scalable to 10 wph by increasing the beam line count up to 13,000.

This FLX-1200, which is being ramped up now, already has shown imaging performances that match its specifications. Full 300mm wafers can be printed in one hour with 32nm half-pitch resolution (**FIGURE 8**). In the IMAGINE program, Leti and its partners are also working to validate a complete turn-key integrated solution allowing fast and secure wafer processing from design to silicon. Such infrastructure developments around data treatment, materials, process, etch and metrology will be required to speed-up the insertion of the MAPPER technology into future production lines.

Leti and MAPPER will demonstrate the operational

FIGURE 7. MAPPER FLX-1200 in Leti cleanroom interfaced with a SCREEN DUO track. Key figures of the tool: Acceleration voltage 5kV; throughput: 1wph with 1,300 beamlines; resolution/alignment specs: 32nmhp / 10nm 3σ.

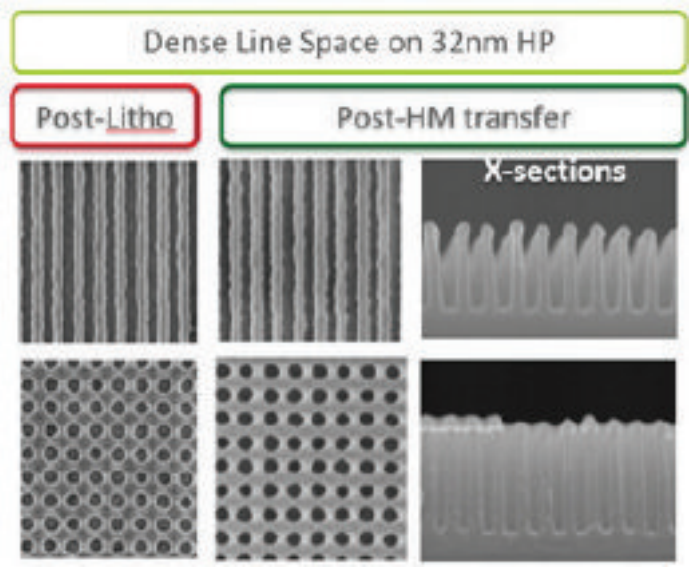

FIGURE 8. First imaging performance of the FLX-1200 on full 300mm wafer

capability of the FLX-1200 in its final configuration, including mix-and-match alignment performances. The achievement of this key demonstration milestone is essential to launching this technology. Then, after final ramp-up, the MAPPER platform is expected to be aligned in terms of specifications with 14nm technology (32nm hp). A wide range of potential applications based on its mask-less concept and throughput potential already have been clearly identified: CMOS prototyping and low-volume production, complementary lithography concept for high-end patterning[6], new industry segments (photonics, low-cost circuit functionalization, large field exposure, etc.).

Nano-imprint lithography

Nano-imprint lithography (NIL) stands out from the other conventional lithography processes (photolithography, electronic lithography, EUV lithography) because of the fundamental mechanism of creating the final structures. In the case of nano-imprint, the flow of the resist directly shapes the pattern through the stamp cavities, eliminating the need for chemical contrast, as is the case for optical lithography resists. In recent decades, significant efforts have been made to extend the distance between the photomask and the resist-coated wafer to reduce defectivity and enhance resolution. Therefore, for many scientists, NIL technology appeared to be a UFO, since the process is based on the intimate contact between the working stamp and the resist to be embossed.

In the past 20 years, significant progress has been made to make the technology more mature and ready for high-volume manufacturing. Among the several existing

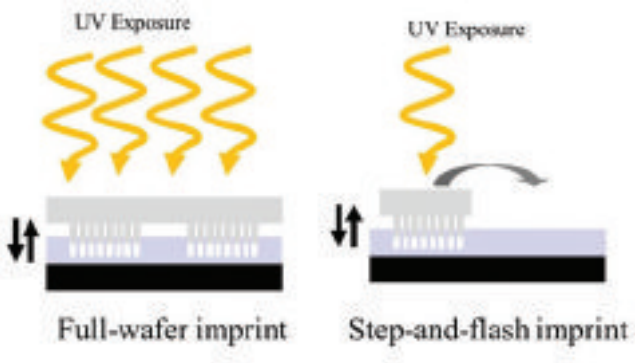

FIGURE 9. Schematic description of the full-wafer and step-and-flash imprint options.

NIL technology alternatives, the UV-based imprint, using transparent stamp, is today the standard one. Two well-established options are now available on the market: the full-wafer imprint (the size of the stamp corresponds to the size of the wafer to be printed) and the step-and-flash imprint in which a small stamp (i.e. die size) is stepped, as in optical lithography across the wafer to be processed (**FIGURE 9**).

If the step-and-flash NIL technology is better suited to address the semiconductor markets (NAND flash memory, DRAM and logic) with its high level-alignment capability and its good control of defectivity density[7], the full-wafer NIL option could quickly become the reference manufacturing option for the emerging and growing markets such as LED and photonics-based devices (**FIGURE 10**).

However, this wafer-scale imprint solution still lacks quantitative data regarding its technology assessment for high-volume manufacturing. Commercial equipment[8] and resists, the cornerstones of this technology, are already available. But some links in the industrial supply chain (design rules, master manufacturing and repair, in-line defectivity and metrology controls, fully integrated process flows) still must be established and qualified to make this technology more mature.

To accelerate adoption of this technology, Leti and EV Group launched in June 2015 a new collaborative industrial program called INSPIRE, aimed at demonstrating the benefits of this full-wafer NIL technology and spreading its use for applications beyond the traditional semiconductor industry. Much more than a classic industrial partnership, the program is designed to support development of new applications from the feasibility-study stage up to the first manufacturing steps,

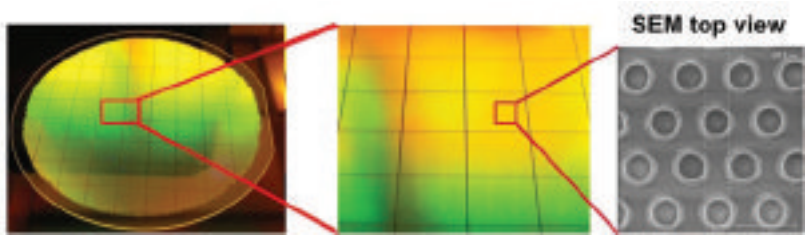

FIGURE 10. Full wafer scale imprinted wafer for photonic crystal application.

including the prototyping phase in Leti's clean room. INSPIRE is also designed to demonstrate the technology's cost-of-ownership benefits for a wide range of application domains. The final objective of this program is to facilitate the transfer of the developed integrated process solutions to industrial partners. The steps should significantly lower the entry barrier for NIL technology and speed up its use in production lines.

Conclusion

The availability of patterning alternatives in the lithography landscape represents a big opportunity to properly address the coming needs generated by the IoT. Besides conventional optical lithography, they offer industry new and/or complementary advantages: innovation capability and opportunities to better manage cost of ownership. But not only that! The high-resolution potential, the ability to facilitate design-innovation validation, and the complementarity of these alternatives with other patterning solutions also highlight their strengths. The step now is to finalize the evaluation of these technologies with respect to industry standards and establish them as real and credible lithography alternatives.

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